1.1 General

Toshiba T1100 PLUS is a portable personal computer which is compatible with IBM PC and is situated at higher rank of portable computer than Toshiba T1100. It provides many powerful functions in spite of its compact size. Hardware of the T1100 PLUS, most of IC chips are C-MOS type so that the power consumption is very little (W) and Gate Array IC chips are applied so that it is very compact and light weight ( ).

The T1100 PLUS System has following two types.
1. F type - Only one Floppy Disk Drive.
2. F/F type - Two Floppy Disk Drives.

The T1100 PLUS is composed of System PCB, Keyboard, LCD, 3.5" FDD (Floppy Disk Drive), Power Supply Unit and case. LCD can display 640 X 200 pixels in graphic mode and 2000 characters in character mode. The 3.5" FDD have capacity of 720KB.
The standerd memory size of the T1100 PLUS is 256 KB and it is able to extend up to 640 KB with optional Memory Card.
Option unit to the T1100 PLUS System are one Memory Card (384 KB), Modem Card and Interface Card are capable to be installed in the T1100 PLUS System Unit. The optional external unit attached to the system unit are 5.25" External FDD 2D (Storage capacity of 360 KB) and I/O Expansion Box are prepared.
The T1100 PLUS has connectors of Color/Monochrome CRT Display port and RS232C port and Printer/FDD on the rear panel of the T1100 PLUS.

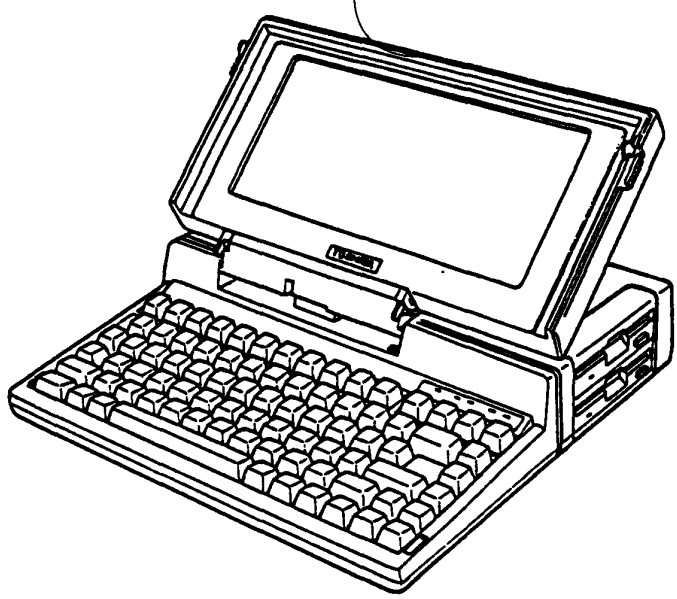
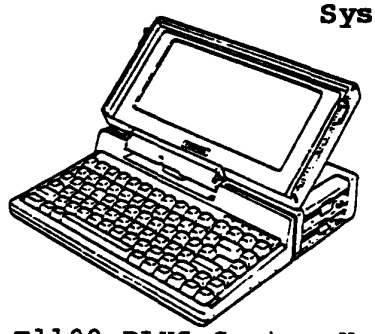


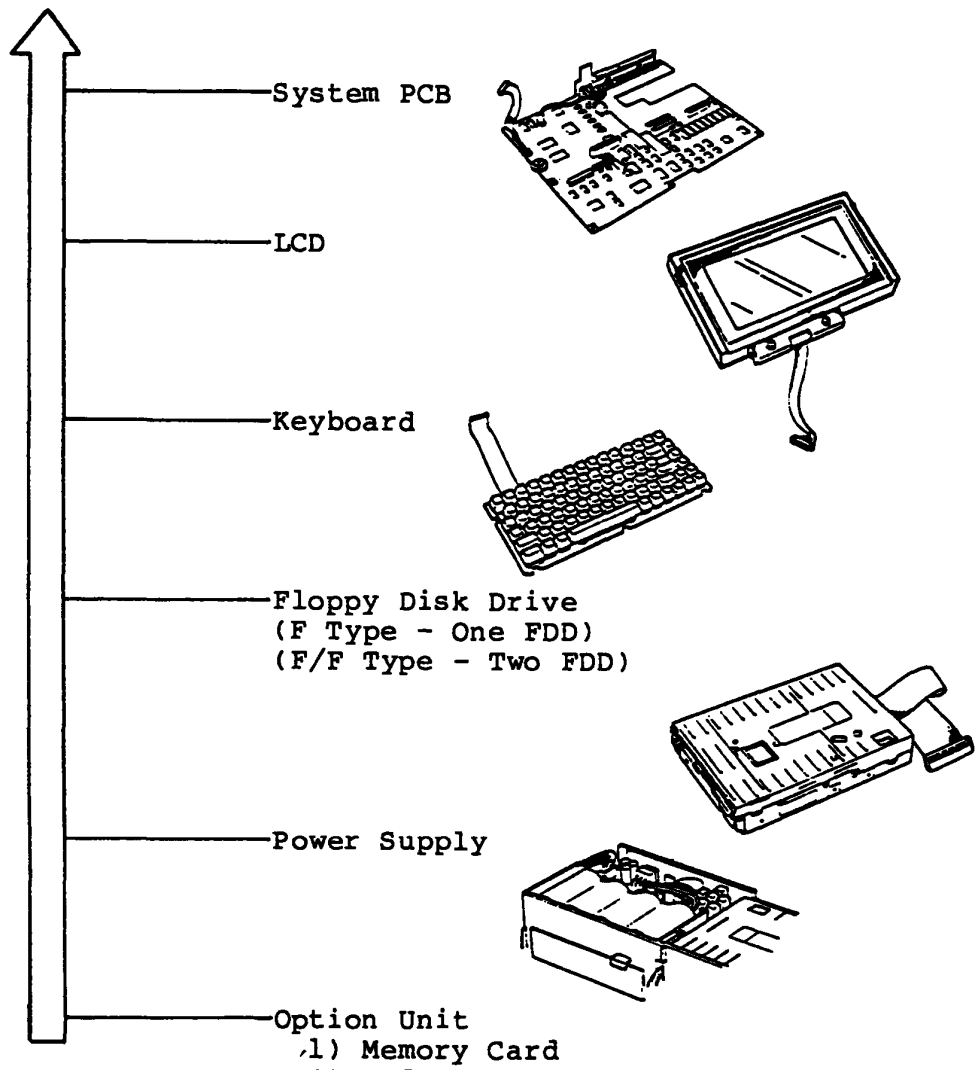
Figure 1-1 T1100 PLUS System

To be continued.

System Configuration



T1100 PLUS System Unit (F Type , F/F Type)



To be continued.

Configuration Matrix

Modules/Units *Subsystem	Standard	Options
System Unit		
* System Board	1	
CPU		
256KB RAM		
Color/Graphics Controller & Interface		
Floppy Drive Controller & Interface		
Parallel Printer Port		
Keyboard Interface		
* LCD (640 x 200 pixels)	1	
* Keyboard (81 keys)	1	
* Floppy Disk Drive (FDD)		
F Type ... One FDD (3.5")	1	1
F/F Type ... Two FDD (3.5")	2	
* Power Supply Unit (Battery and PCB)	1	
* Upper Cover		1
* Lower Cover		1
Memory Expansion Card (384 KB)		1
Modem Expansion Card		1
I/O Expansion Box (and Interface Card)		1
External Floppy Disk Drive (5.25") 2D		1

1.2 System Unit

The T1100 PLUS System Unit is composed of subunits. All subunits of T1100 PLUS system are built in one compact System Unit case. They are System PCB (Printed Circuit Board), 3.5" FDD (Floppy Disk Drive), LCD (Liquid Crystal Display), Keyboard, Power Supply Unit, Speaker and harnesses.
In a maintenance service, the faulty subunit will be replaced with good spare subunits easily.
Followings are showing locations of subunits of the T1100 PLUS System Unit.

(1) Locations of subunits

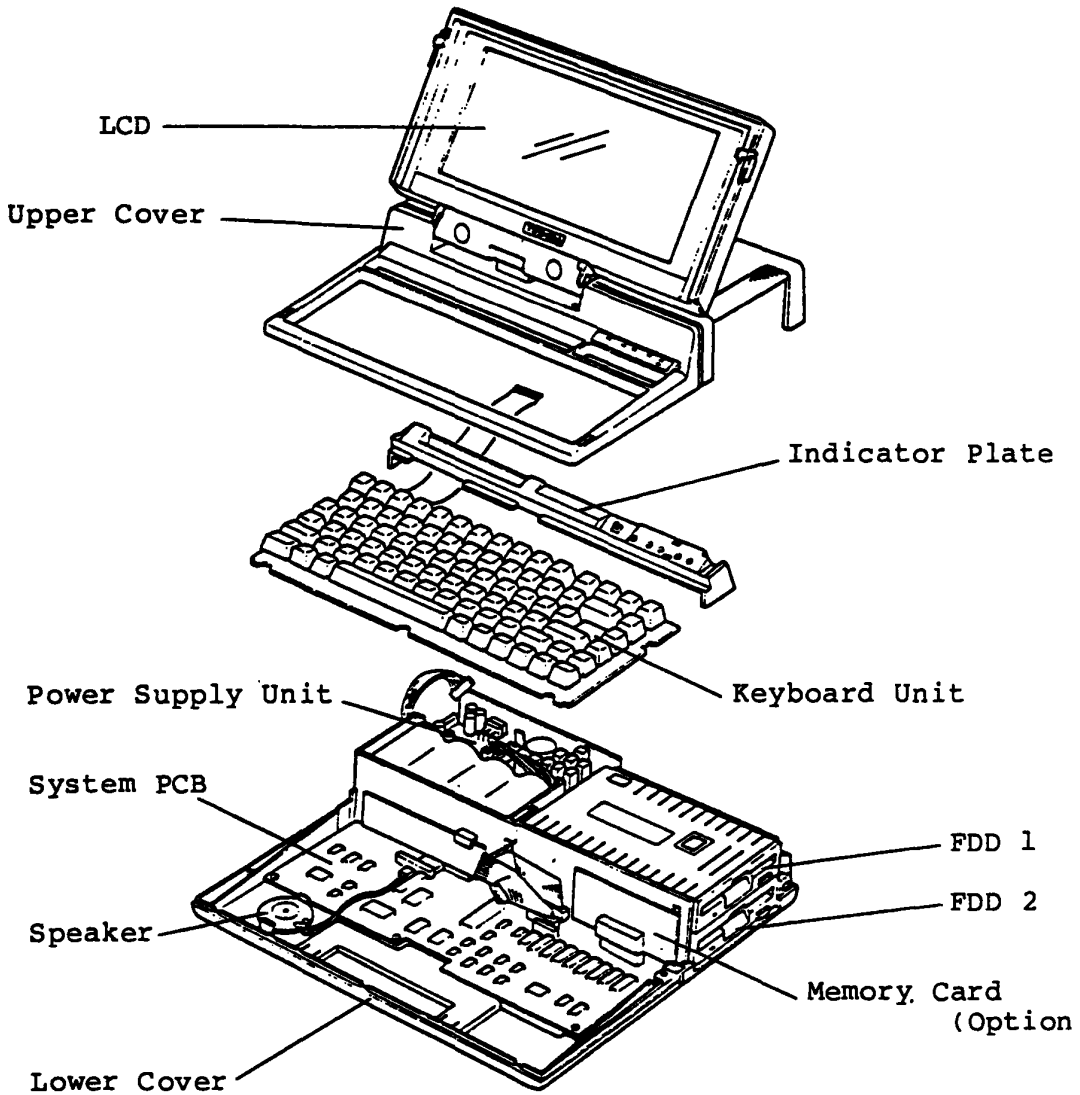


Figure 1-2 System Unit(F/F Type)

To be continued.

The System Unit contains the following subunits.

System PCB
3.5" FDD (Floppy Disk Drive)
LCD
Keyboard
Power Supply Unit
Harnesses
Covers

Ac Adaptor is used for rechargment of the Battery and/or power source to the T1100 PLUS System indoors by plug in the DC Jack on the back of the System.

AC Adaptor 120 108 132
Input : ~~115~~V (~~104~~-~~127~~V) For U.S.A. version
230V (207-253V) For Europe version
Output : 9V DC

(2) Locations of connectors and switches

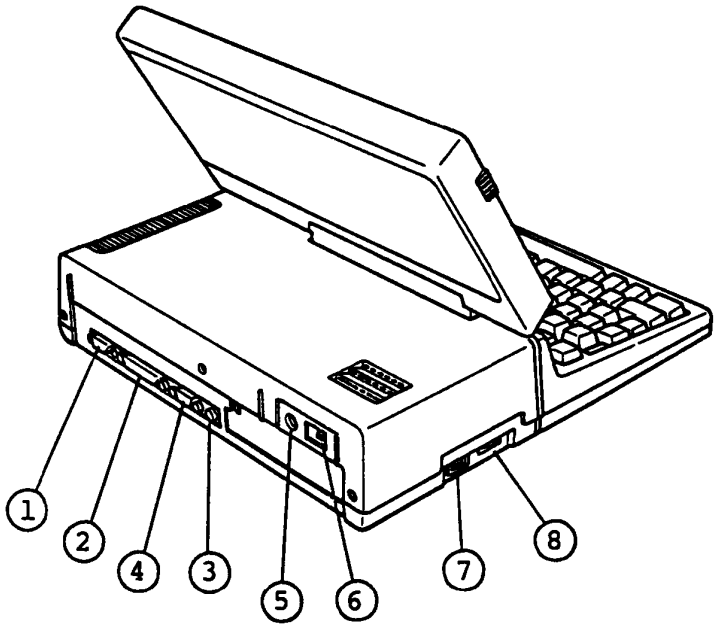


Figure 1-3 Rear View of the T1100 PLUS

① : RS-232C Connector
② : External FDD and Printer Connector
③ : Monochrome CRT Display Connector (Composit)
④ : Color CRT Display port (RGB)
⑤ : DC jack
⑥ : Power Switch
⑦ : PRT/FDD Select Switch
⑧ : LCD CONTRAST Dial

1.2.1 System PCB

System PCB is composed of processor (i80C86-2), RAM Memory (256KB for Main Memory, 32KB for Video RAM), ROM Memory (32KB for BIOS, 32KB for Character Generater of CRTC), FDD Controller, Keyboard Controller, Display and Printer controller and Printer Adaptor.
As the advanced technology, this PCB introduces four "Gate Array" packages .

The System PCB houses:

- Central Processor Unit (CPU; i80C86-2 compatible 16-bit Processor.)
  Clock speed is 4.77 MHz (Slow mode) or 7.16 MHz (Fast mode).
  Switching the clock speeds can be done by depressing some keys of keyboard.
  When the system power turns on, the processor runs at 7.16 MHz.

- Main Memory 256KB dynamic RAM (as standard configuration)

- PCB connector for additional Main Memory (from 256KB to 640KB)
  Internal 384 KB memory expansion cards.(Option)

- BIOS ROM (256K ~~Bytes~~ 32KBy bits MASK ROM) including Initial Reliability Test and Initial Program Loader.

- Programmable Interrupt Controller (PIC; i82C59A compatible)
  Providing eight-level Interrupt Register/Priority Logic, Interrupt Mask and Vector Address

- Programmable Interval Timer (PIT; i82C53 compatible)

- Direct Memory Access Controller (DMAC; i82C37 compatible) for Floppy Disk Controller, Hard Disk controller and serial Input/Output operation.

- Floppy Disk Controller (FDC : TC 8565F compatible)

To be continued.

The System PCB houses (Continued):

- Calender Clock (Clock : TC8250 compatible)

  Calender Clock power are supplyed from the Ni-Cd battery unit. Battery (Ni-Cd) life lasts for about five years (dealer replacable). When the power of the system turns on, this battery is charged.
  (NOTE)
  If you haven't used the system unit for tow months since battery has been charged, the stored data disappears.

- Universal Asynchronous Receiver Transmitter
  (UART for RS232C port : 82C50 compatible)

- Keyboard controller (80C49A compatible)

- DIP switch (Configuration information for Software)

- Parallel 8-bit Printer Interface port (Centronics Interface)

- BUS Controller Gate Array
  (Bus control, Keyboard control, etc.)

- BUS Driver Gate Array

- I/O Decorder Gate Arrey

- Display Controller Gate Array
  (LCD, RGB-CRT, Monochrome-CRT, Composit signal control)

To be continued.

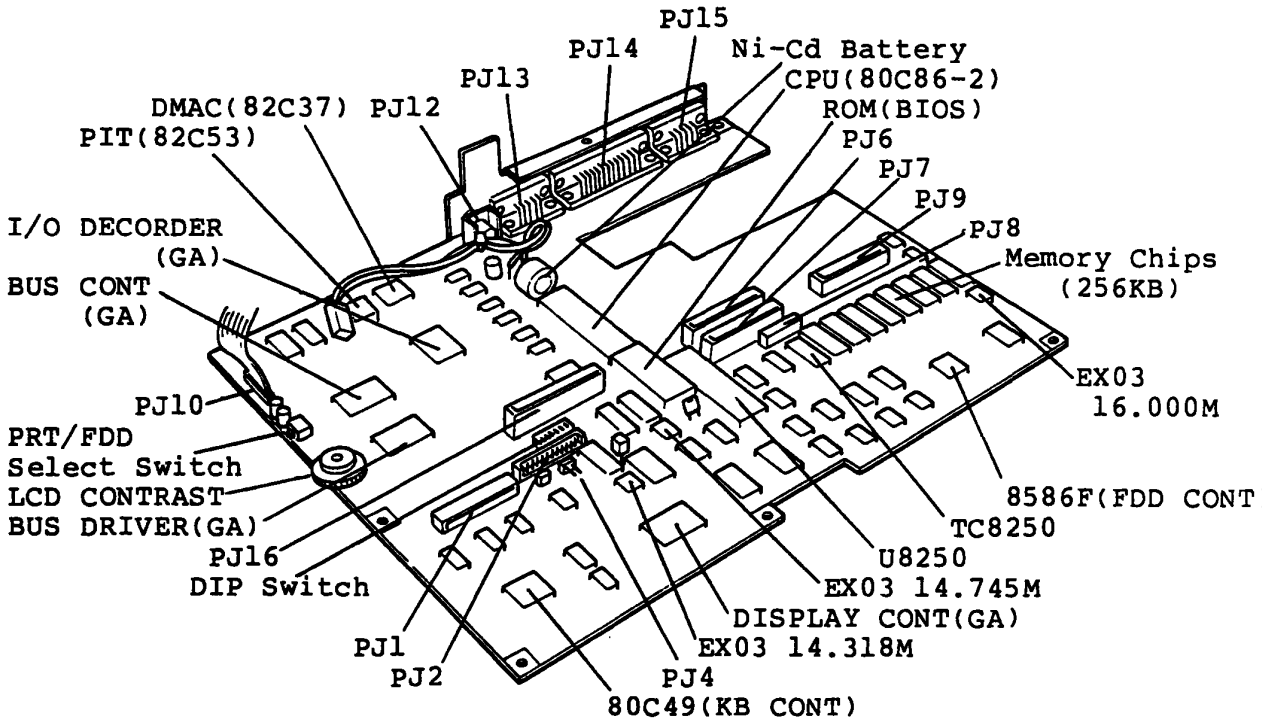


Figure 1-4 System PCB

Connectors

PJ1 - Keyboard Connector
PJ2 - LCD Connector
PJ4 - Speaker Connector
PJ6 - FDD 1 Connector
PJ7 - FDD 2 Connector
PJ8 - LED Connector
PJ9 - Expansion Memory Card Connector
PJ10 - Power Supply Connector
PJ12 - Composit Video Connector
PJ13 - Color CRT Display Connector
PJ14 - External FDD and Printer Connector
PJ15 - RS-232C Connector
PJ16 - Expansion BUS Connector

To be continued.

Configuration switches

The T1100 PLUS System Unit Configuration Swicth is 6 pin Dual-In Line Package (DIP) switches.

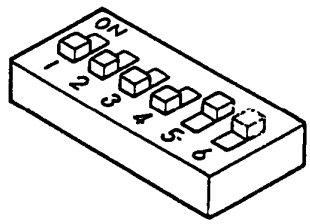


Figure 1-5 DIP switch

The meanings of all Configuration DIP Switch's settings are described in the following table.

SW	DESCRIPTION
1	Should be always OFF
2,3	Amount of Memory System Board SW2,SW3 ON ON ... 256 KB OFF ON ... 384 KB ON OFF... 512 KB OFF OFF... 640 KB
4	Number of 3.5" drives ON ..... One Floppy Disk Drive OFF ..... Two Floppy Disk Drive
5	This is the switch to set port address of RS232C on the system board and I/O port address of modem card (option) of I/O expansion slot. ON ..... I/O address of RS232C port → COM-1 I/O address of modem port → COM-2 OFF..... I/O address of RS232C port → COM-2 I/O address of modem port → COM-1
6	Enable/Disable Display Controller ON ..... Enables the Display Controller on the System Board. OFF..... Disables the Display Controller on the System Board.

1.2.2 3.5" Floppy Disk Drive (FDD)

The SMD-280L of 3.5" FDD is a high performance, high reliable, slim sized Floppy Disk Drive (FDD) for 3.5" floppy disks.
The drive is able to read and write single or double density 3.5" floppy disk with 1M-bytes of recording capacity (unformatted) in double side, double density and 135 TPI.

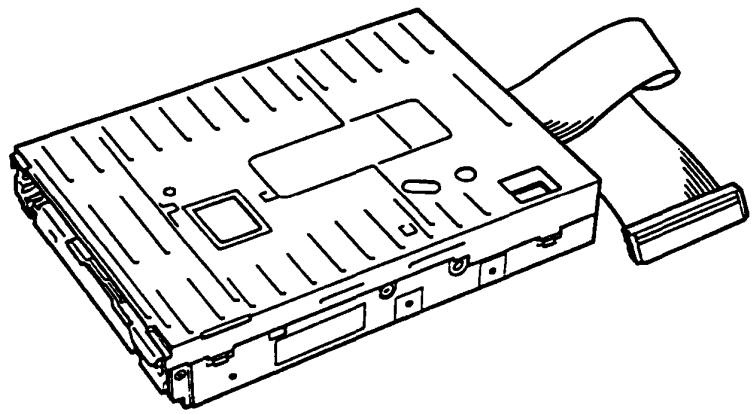


Figure 1-6 3.5"FDD

Performance Specification

Storage Capacity (K-bytes)	
Unformatted	1,000
Formatted	720
Number of Heads/Drive	2
Track/Surface (tracks)	80
Data Transfer Rate (K-bits/Second)	250
Access Time (ms)	
Per Track	6
Average (Including Settling Time)	100
Settling Time	15
Head Load Time	0 *(1)
Average Latency Time (ms)	100
Recording Density (Max.)	
Bit Density (BPI)	8,717
Track Density (TPI)	135
Motor Start Time (ms)	500
Rotational Speed (RPM)	300
Recording Method	MFM
Recording disk	3.5" ANSI Standard disk
Weight (g)	460
Size (mm)	101.6(W) X 149.5(D) X 25.4(H)

Note *(1) : Heads have been always loaded in operation mode.

1.2.3 Keyboard

The keyboard consists of 81 keytops crresponding number of Keyswitches (81) and matrix circuit, and it is connected to the System PCB through signal cable.
The keyboard controller (80C49A) is built in on the System PCB. It is applied by changing the keytops with option keytops for character differences due to the Nations where the T1100 PLUS is used

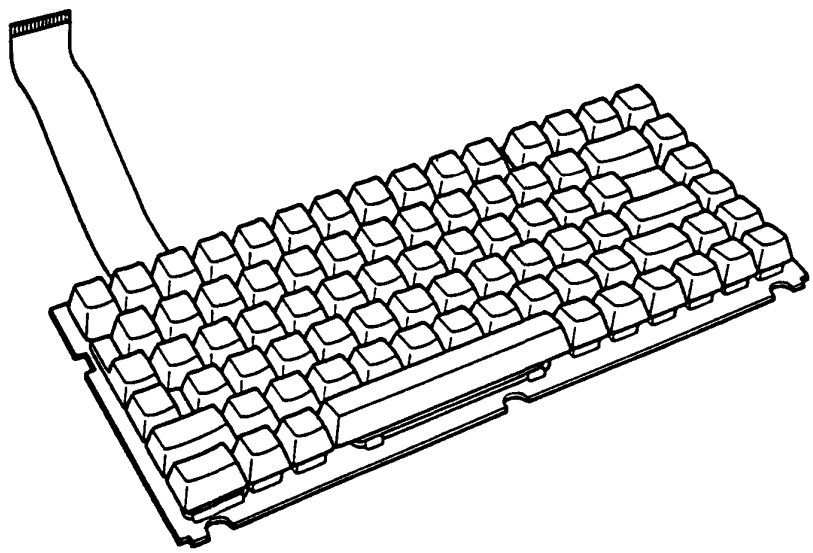


Figure 1-7 Keyboard

1.2.4 Liquid Crystal Display

The LCD Module (~~TCL~~ LC-365-121) is flat panel 640 x 200 pixels Liquid Crystal Display unit with aspect ratio of the active area of four to three.
The LCD can display graphic patterns, numerals, alphabets and symbols up to 2,000 charactors (8 x 8 dots charactor).

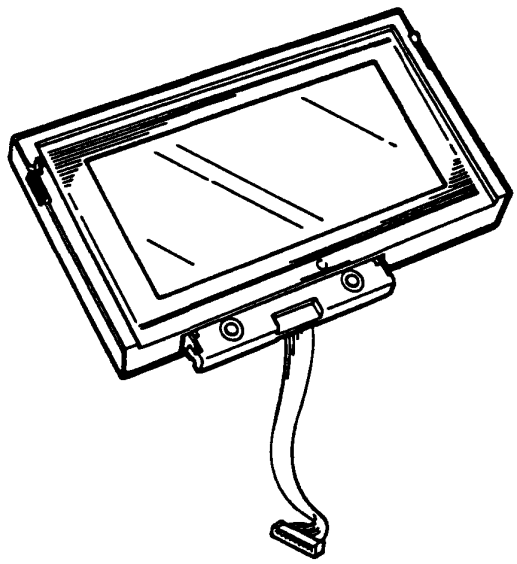


Figure 1-8 LCD

Clock (~~Hz~~ MHz)	2.2
Supply Voltage (volts)	+5V DC ± 0.5V -15V DC ± 0.5V
Number of Dot (pixel)	640 (Horizontal) 200 (Vertical)
Number of Characters (Dot)	80 X 25 (2000 characters) (8 X 8 dot format)
Dot Size (mm)	0.46 H X 0.32 W
Dot Pitch (mm)	0.35 (Horizontal) 0.49 (Vertical)
Power Consumption (mW)	400
Size (mm)	275.0 X 126.0 X 15.8
Weight (g)	500

1.2.5 Power Supply Unit

The Power Supply Unit of the T1100 PLUS System Unit is housed Power Supply PCB and it furnishes DC power, +5, +9, -9 and -15 volts for all components in the T1100 PLUS System Unit. These power are supplyed from the Ni-Cd battery Unit or AC Adaptor.

This Power Supply Unit is Housed in System Unit and is designed to support the following:

1) System PCB
2) 3.5" FDD
3) LCD
4) Expansion PCB's

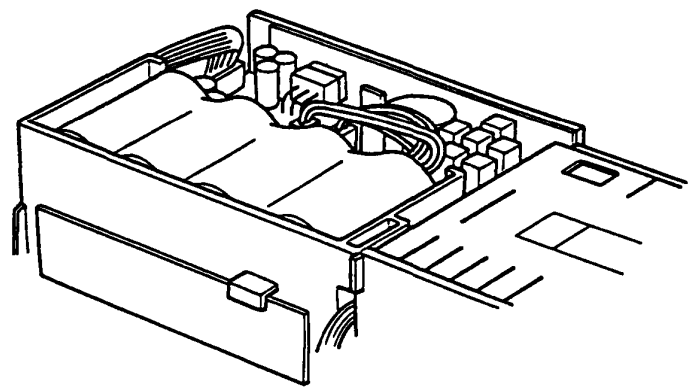


Figure 1-9 Power Supply Unit

Input (DC)	+ 5V (from Battery Package)
Output (DC)	- 9V ( ) 30mA + 9V ( ) 10mA -15V ( ) 13mA + 5V ( ) 1.5A

1.3 Option Units

The T1100 PLUS has a variation of option units to be attached to the system. Following Units are possible to attached to the T1100 PLUS system.

1) Memory Expansion Card (384KB)

2) Modem Expansion Card

3) I/O Expansion Box and Interface Card

4) External Floppy Disk Drive (5.25") 2D

1.3.1 Memory Expansion Card

The Expansion Memory Unit is an option memory board to be installed on the System PCB. It is installed to the T1100 PLUS System Unit just by plugging in the connector on the System PCB and expands the memory size of the T1100 PLUS system till 640KB with the basic 384KB memory.
When the Expansion Memory Unit is installed, the Configuration DIP Switch must be changed properly. (Refer to page 1-10)

WARNING

The Memory chip is very weak in a static electricity shock. When you handle the Expansion Memory board itself, it is recomended to protect the Expansion Memory Unit with anti static electricity materials.

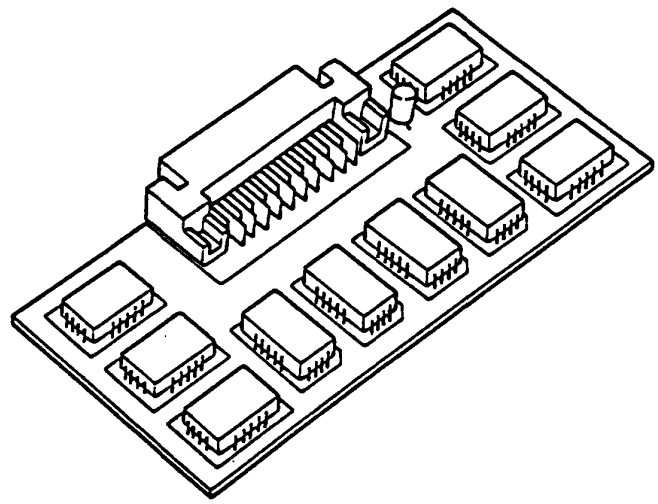


Figure 1-10 Expansion Memory Unit

1.3.2 Modem Expansion Card

The Expansion Modem Card is an option card which communicates with an external asynchronous communications device through an appropriate cable having modulatar jacks on both end. one end of the cable is connected to the External Modem Card and other end is to a wall jack of the telephone line.

It supports CCITT V.22 asynchronous mode and BELL 212A. The specifications of this card are as follows.

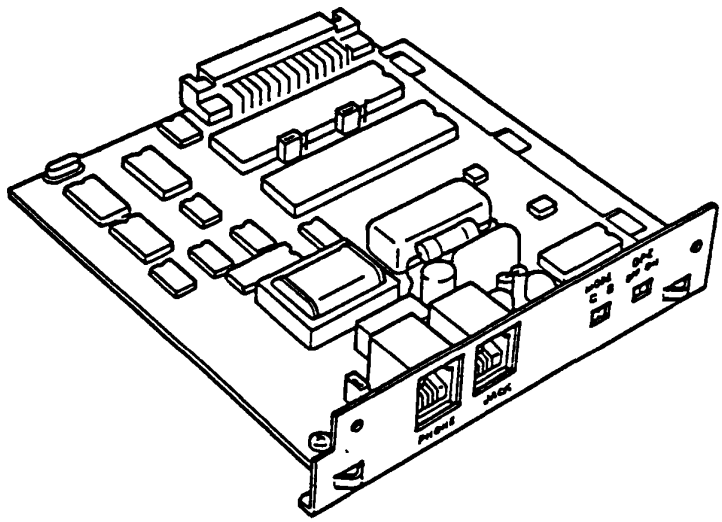


Figure 1-11 Modem Expansion Card

Performasce Specification of Modem Card

Data Format Low Speed(0-300 BPS)	7 or 8 bits, 1 or 2 stop bits odd, even or noparity.
High Speed(1200BPS)	7 bits, no parity, 2 stop bits 7 bits, e/o parity, 1 stop bits 8 bits, no parity, 1 stop bits
Dialing Capability	Tone Dial / Pulse Dial
Audio Monitor	Speaker
Receive Sensitivity	-45dBm

1.3.3 I/O Expansion Box and Interface Card

Expansion Box is an option unit to provide the I/O channel to the T1100 PLUS System. This unit is composed of the Expansion I/O Cable, Interface Card, Expansion Box and AC Power Cord. The Expansion Card, Backpanel Card and Power Supply are in the Expansion Box. Adding an Expansion Box provides five expansion slots.

An option adaptor in the Expansion Box and the System Unit communicates through the Interface and Expansion Cards. The Interface Card is plugged into the EXP sockets at the rear of System Unit. This card is connected to the Receiver Card in the Expansion Box via a cable having 62-pin D-shell connectors at the both ends. The Expansion Card is mounted one of six Expansion Slots in the Expansion Box.

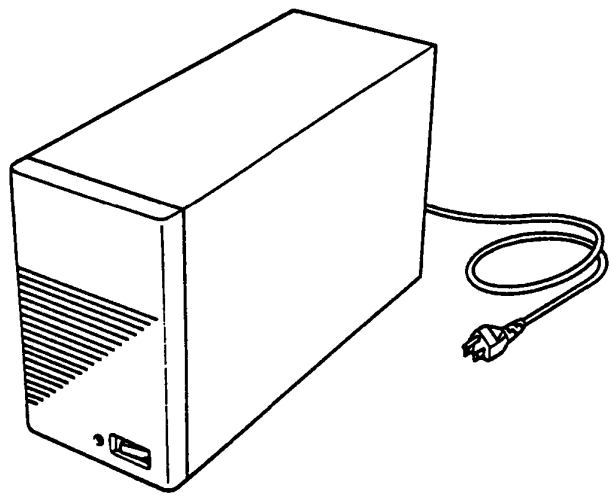


Figure 1-12 Expansion Box

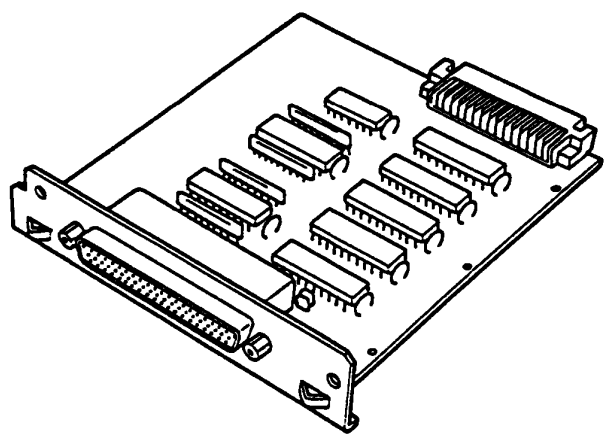


Figure 1-13 Interface Card

1.3.4 5.25" External FDD (SD-521)

The SD-521 is a high performance, high reliable, slim sized Floppy Disk Drive (FDD) for 5.25" floppy disks.
The drive is able to read and write single or double density 5.25" floppy disk with 500KB of recording capacity (unformatted) in double side, double density and 48 TPI.
T1100 PLUS System uses the SD-521 as external 5.25" FDD unit (option).

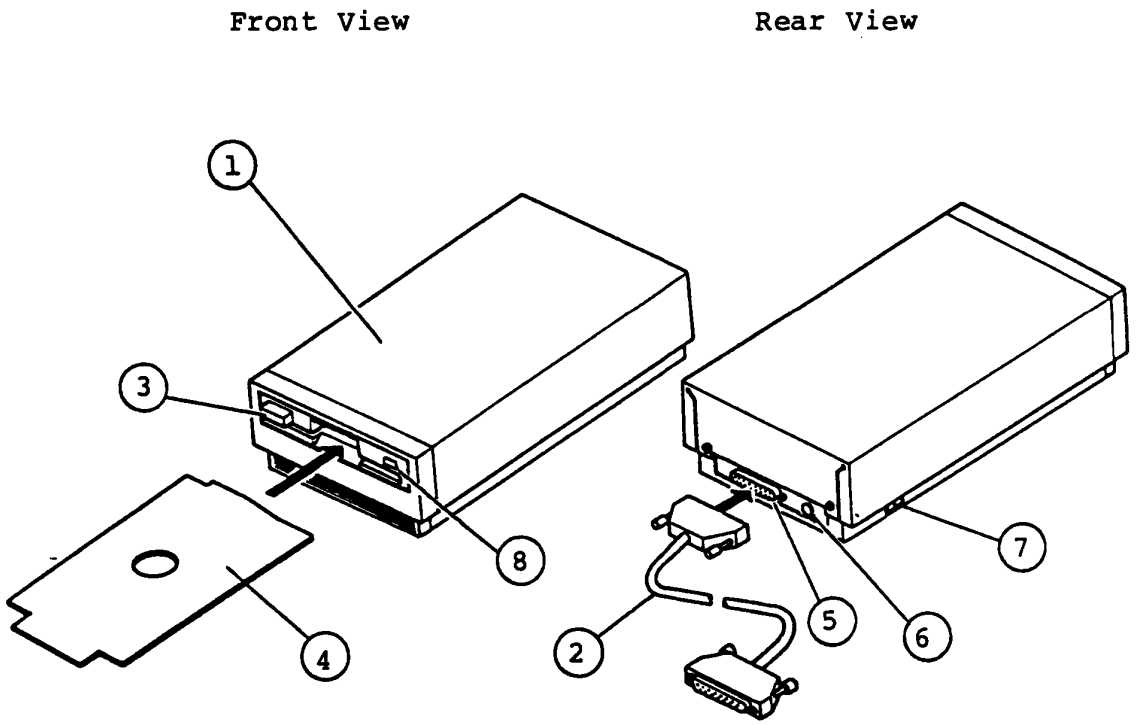


Figure 1-14 5.25" External FDD (SD-521)

Explanations on components

(1) 5.25" External FDD
5.25" External FDD (Floppy Disk Drive) is composed of Disk Drive and Control PCB.

(2) Connector Cable
This cable is a signal cable between the FDD and the T1100 PLUS System Unit.

(3) Disk Eject Button
This button is used to remove a Floppy Disk from the FDD .

(4) Cardboard Protector
This cardboard is used for head protection against a shock during a transportation of the FDD.

(5) Dsub-Connector
The Dsub-Connector is a 25-pin connector for the Connector Cable.

(6) DC Jack
The DC Jack is for connecting the AC Adaptor.
The required specification of AC Adaptor is
Input : 220-240V ac
Output : 18V dc, 600mA

(7) Power Switch
Push the rear portion of the switch to Power ON.
Push the front portion of the switch to Power OFF.

(8) Drive Unit Select Indicator
It is lit while the FDD is selected to use by The T1100 PLUS system. Do not eject a disk while it is lit.

Performance Specification of SD-521

Storage Capacity (K-bytes)	
Unformatted	500
Formatted (9 Sectors/Track)	360
Number of Heads/Drive	2
Track/Surface (tracks)	40
Data Transfer Rate (K-bits/Second)	250
Access Time (ms)	
Per Track	6
Average	97
Settling Time	15
Head Load Time	0
Recording Density (Max.)	
Bit Density (BPI)	5,876
Track Density (TPI)	48
Motor Start Time (s)	0.5
Rotational Speed (RPM)	300
Recording Method	MFM

1.4 CRT Display Interface Connector

The T1100 PLUS system has CRT Display Interface connector on the back of T1100 PLUS System Unit.
You can connect the following types of CRT Display to the T1100 PLUS System Unit.

1) Medium Resolution Color Display Unit

   320 x 200 pixel's Color CRT Display.
   It can display 80 column x 25 line or 40 column x 25 line characters in character mode on one frame.
   It can be connected to the T1100 PLUS System through D-sub 9-pin connector.

2) Low Resolution Monochrome Display Unit

   640 x 200 pixel's Monochrome CRT Display.
   It can display 640 x 200 pixel graphic pattern.
   It can display 80 column x 25 line or 40 column x 25 line characters in character mode.
   It connected through phone jack.

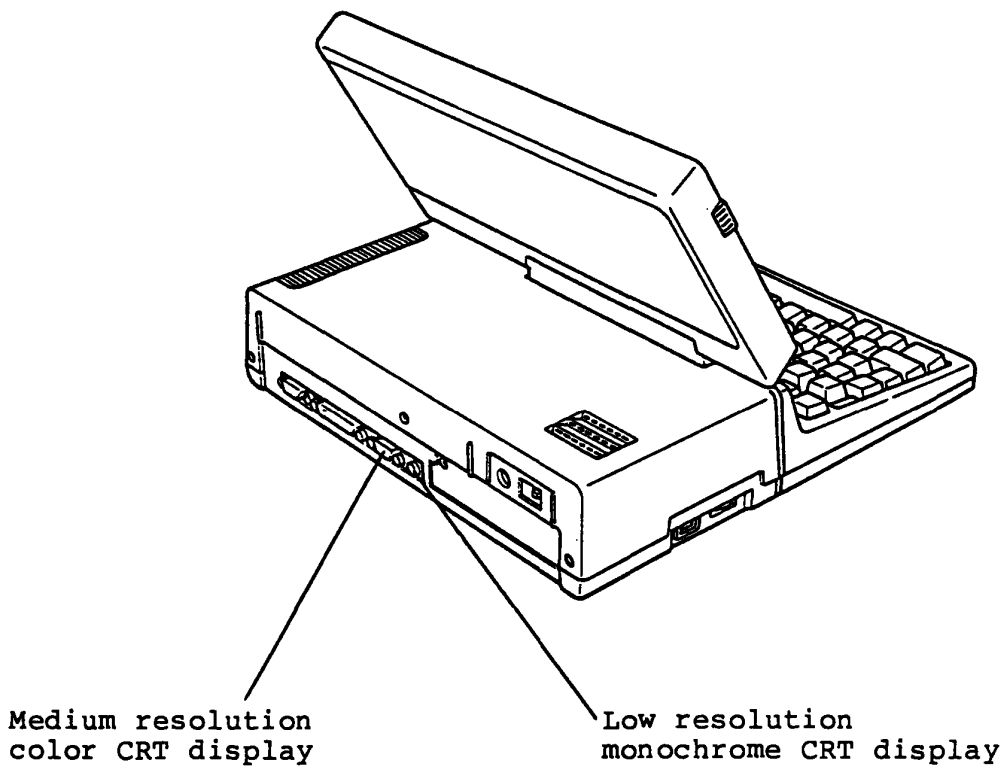


Figure 1-18 Rear View of T1100 PLUS System Unit

Specification

Unit type		
	Signal	Description
1.Medium Resolution Color Display Unit		
	Connector	9-pin D-sub
	Video signal	14.3 MHz (Max) Red video : Positive level TTL compatible Green video: Positive level TTL compatible Blue video : Positive level TTL compatible
	Vertical drive	60 Hz refresh rate 200 scan lines displayed (non-interlace) Positive level, TTL compatibel
	Horizontal drive	15.75 KHz scan rate 320/640 pixels displayed Positive level, TTL compatible
2. Low Resolution Monochrome Display		
	Connector	Phone Jack type
	Video signal	14.3 MHz (Max.) Positive level (1.5v peak to peak)
	Vertical sync	60 Hz refresh rate 200 scan lines displayed (non-interlace) 524 scan lines interlaced total
	Horizontal sync	15.750 KHz scan rate 320/640 pixels displayed

This PART is a Trouble Isolation Procedures (TIP's) for the T1100 PLUS system .
It is based on the FRU (Field Replaceable Unit) which is defined in **PART 7.** The target of this Trouble Isolation Procedures is to isolate the faulty unit from the system and replace it in the field.

The required tools for this trouble-shooting are as follows.

1). MS-DOS System Disk (including T&D program)

2). Work Disk (for FDD test)

3). AVO meter

4). Cleaning Disk

5). Screwdrivers (Blade screwdriver and Phillips screwdriver)

6). Printer port LED

7). Printer Wraparound Connector

8). RS-232C Wraparound Connector

For the trouble-shooting, you are required to read the T&D operation procedure of **PART 8** of this manual.

You will follow the Trouble Isolation Procedures (TIP's) to isolate the failing Field Replaceable Unit (FRU) in case you met a failure on the FRU of the TOSHIBA Personal Computer T1100 PLUS. The TIP's are composed of the following groups, and the TIP's in these groups will lead you to failing FRU.

The [ENTRY] is the isolation procedure of which TIP should be taken for the trouble.
Another TIP's are of the units which will be given by [ENTRY], or the suspected units.
Start from next page, for any trouble shooting.

Fault Component (FRU) is identified already ?

1. If fault component (FRU) is identified already, or obvious problem such as unusual noise or damaged part on a component, go to the appropriate TIP (Trouble Isolation Procedure).

TIP	Page
Power On Diagnostic	4-14
Power Supply Unit	4-12
System PCB	4-24
FDD (3.5" Int. FDD)	4-31
Keyboard	4-54
LCD	4-62
External FDD	4-80

2. If fault component (FRU) is not identified, go to next page.

Before the Trouble Isolation Procedure

Set up the system to standard for checking.

1. Turn OFF the power switch of the System Unit.
2. Discnnect the all connectors from rear panel.
3. Check that the PRT/FDD select switch at the left side (from the view point where you are facing the LCD) of the System Unit is set to PRT side.
4. Rotate the LCD CONTRAST Dial fully to the direction of "High".
5. Release the latches by sliding them forward, hold the latches and pull up the display, then open the LCD.
   And go to **Enter-1.**

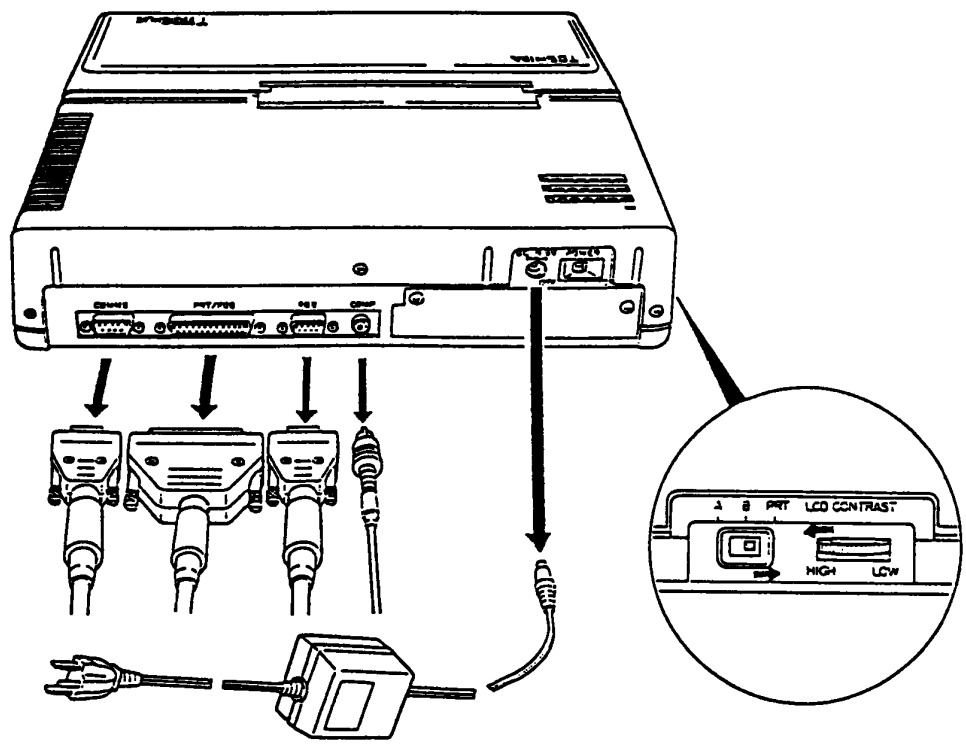


Figure 4-1 Before the Trouble Isolation Procedure

LED check

1. Turn ON the power of System Unit.
2. Check that the LED (Power/Speed) of indicator lighting.

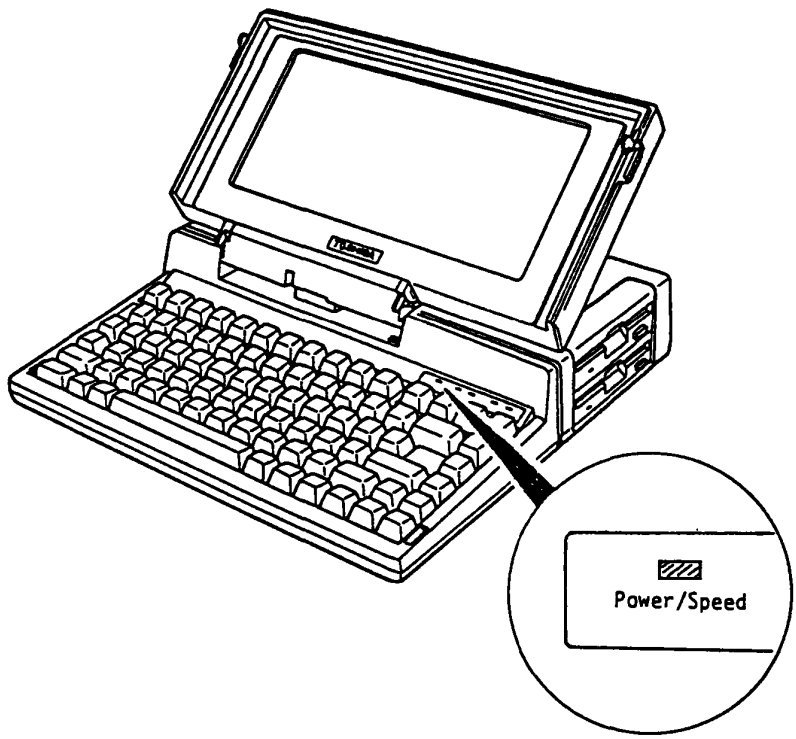


Figure 4-2 LED Check

Is the LED lighting ?

Yes: Go to **ENTRY-2.**

No: Go to **POWER.**
If you have disassembled the System Unit before, confirm that the Indicator cable is connected correctly to the System PCB (PJ8). (refer to PART 5)

LCD check

1. Check that the display indicats all dots for a second momentarily after turning the power ON.

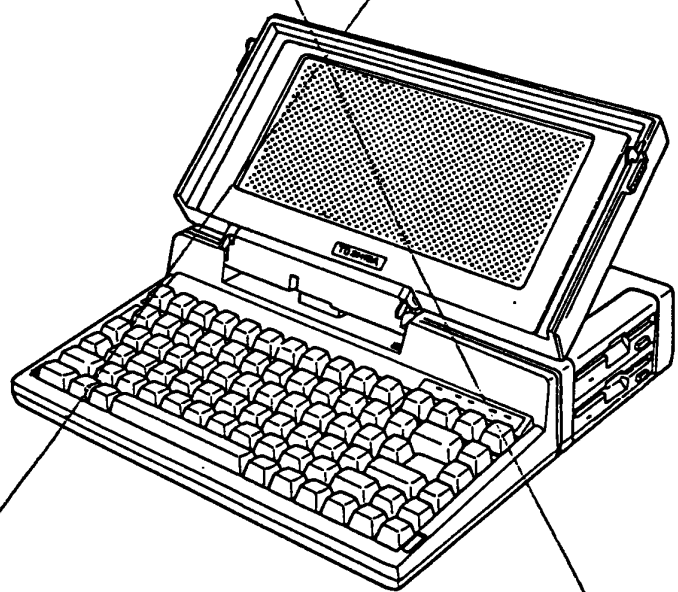


Figure 4-3 Display indicats all dots

Are the above all dots displayed ?

Yes: Go to **ENTRY-3.**

No: The LCD may be faulty.
Go to **LCD.**

Screen check at the start up time

1. Confirm that the following message appears on the display screen.

MEMORY TEST XXX KB

Does the above message appear ?

Yes: Go to **ENTRY-4.**

No: The System PCB may be faulty.
Go to **SYSTEM PCB.**

Speaker check

1. After **MEMORY TEST XXX KB** message appears on the display screen, check that Beep sound from speaker.

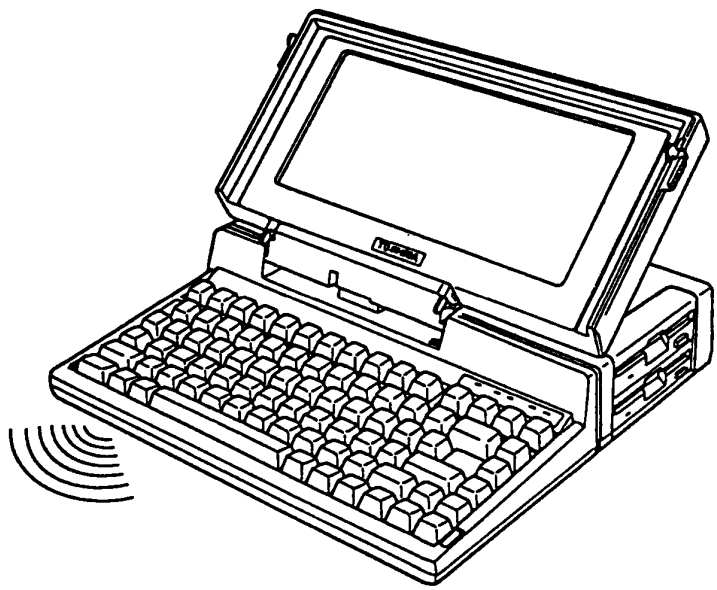


Figure 4-4 Check the beep sound

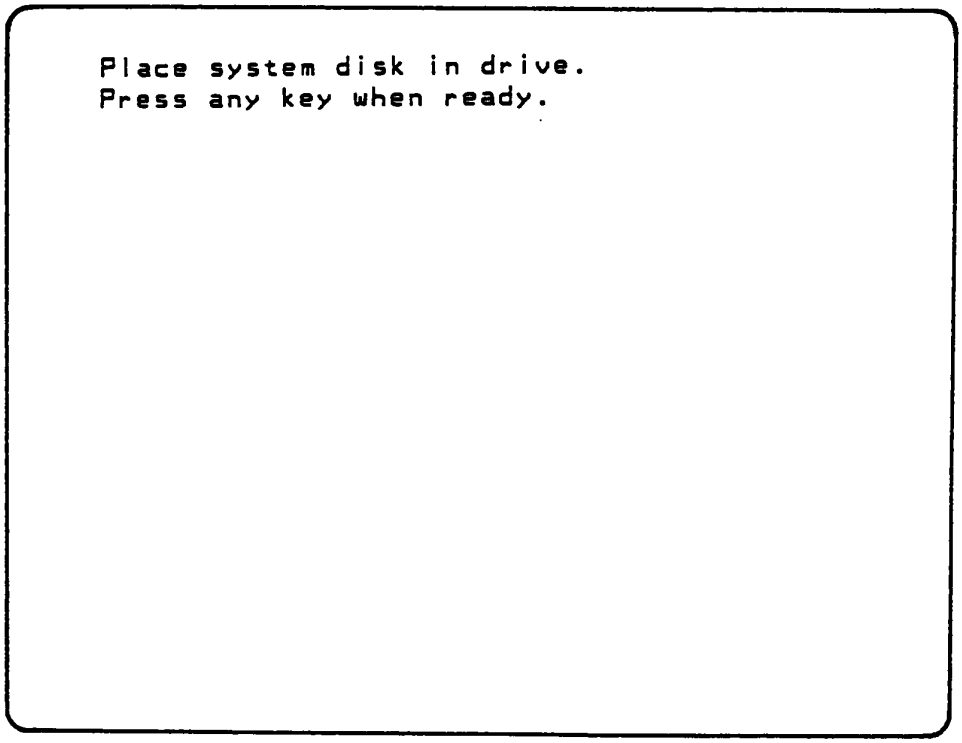
Is the speaker Beep sound ?

Yes: Go to **ENTRY-5.**

No: Turn OFF the power switch of the System Unit.
Confirm that the Speaker cable is connected to the System PCB. (refer to PART 5)
If the Speaker cable is connected to System PCB, replace the Speaker Unit with a good spare Speaker Unit.(Refer to PART 5)
If the failure remains, the System PCB may be faulty.
Go to **SYSTEM PCB.**

Message check

1. Confirm that the following message appears on the display screen, about 15 seconds after the Beep sound from the speaker.



Does the above message appear ?

Yes: Go to **ENTRY-6.**

No: System PCB may be faulty. Go to **FDD.**
Note: If the MS-DOS system disk has been inserted in the FDD before the power ON, the above massage is bypassed. (Go to **ENTRY-6**)

MS-DOS loading cheak

1. Insert the MS-DOS system Disk into the internal disk drive and press the any key.
2. After the MS-DOS loading, press the "ENTER" key twice.
3. Confirm that the following message appears on the display screen.

```
Toshiba  Personal Computer   (R2100EN)      Preliminary version

Copyright 1984,86 Toshiba Corporation

MS-DOS   Ver 2.11
Copyright 1983,84 Microsoft Corp.

Command  Ver 2.11V
Current date is  Wed  1-01-1986
Enter new date :
Current time is   0:36:46.00
Enter new time :

A>
```

Does the above message appear ?

Yes: Go to **ENTRY-7.**

No: You may use a damaged MS-DOS System Disk.
Replace the good MS-DOS System Disk, then repeat the operation to verify it.
If failure remains, the Floppy Disk Drive may be faulty.
Go to **FDD.**

Input check

1. Input file name of **CE DIAGNOSTIC** as **testce** to load the diagnostic program.
   The underlined position on the follow screen are to input **testce** message.

2. Confirm that the **testce** message is inputed on the screen.

```
Toshiba  Personal Computer  (R2100EN)      Preliminary version

Copyright 1984,86 Toshiba Corporation

MS-DOS   Ver 2.11
Copyright 1983,84 Microsoft Corp.

Command  Ver 2.11V
Current date is  Wed  1-01-1986
Enter new date :
Current time is   0:36:46.00
Enter new time :

A>testce
```

Is the message inputed ?

Yes: Press the "ENTER" key.
Execute the T&D operation. (Refer to PART 8)

No: Go to **KEYBOARD.**

This section describes how to execute the **POWER-ON DIAGNOSTIC TEST** .

You need to prepare the Printer Port LED (maintenance tool).

POWER ON DIAGNOSTIC TEST is for executing System PCB test.

Go to **POWER-ON DIAGNOSTIC-1** .

Set the Printer Port LED

1. Turn OFF the power switch of the System Unit.
2. Disconnect the all cables from the System Unit of rear panel.
3. Connect the Printer Port LED (A) (Maintenance tool) to PRT/FDD connector (B) of the System Unit (rear panel) as shown below.
4. Confirm that the PRT/FDD select switch (C) is set to PRT side.

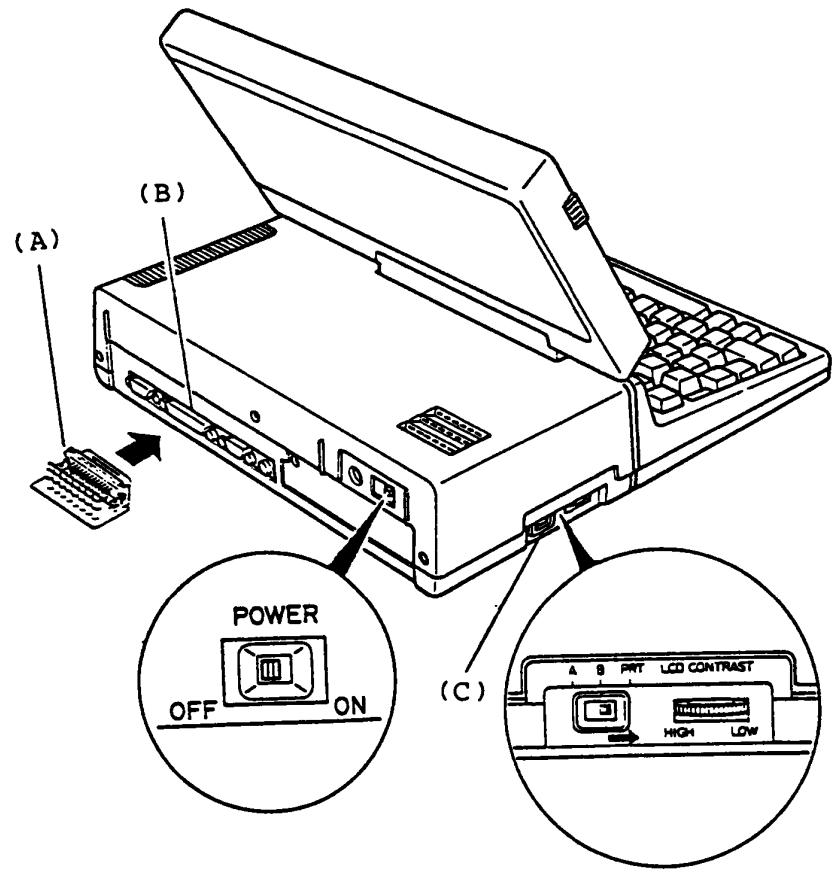


Figure 4-5 Printer Port LED Setting

Run the Power-On Diagnostic

1. Turn ON the power switch of the System Unit to run the Power-On Diagnostics.
2. Confirm that the LED of Printer Port LED is lighted.

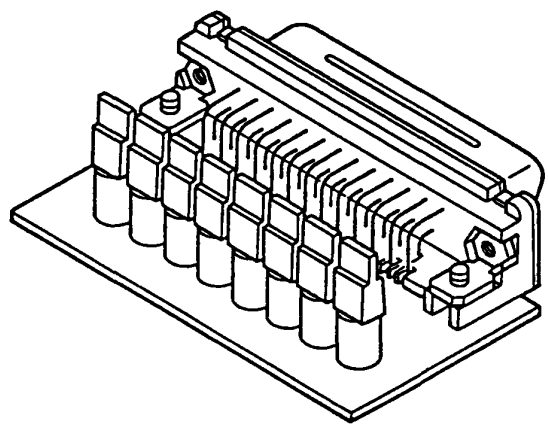


Figure 4-6 Printer Port LED

Is the Printer Port LED lighted ?

Yes: Go to **POWER-ON DIAGNOSTIC-3.**

No: Go to **POWER.**

Read error status and isolate the failre component.

You may have an error condition in the Power-On Diagnostics, and the status has been indicated on the Printer Port LED.
(NOTE) The status **D5(H)** means no error.

1. Read the error status on the Printer Port LED.

2. Isolate the failure component in accordance with the following chart of Power-On Diagnostics.

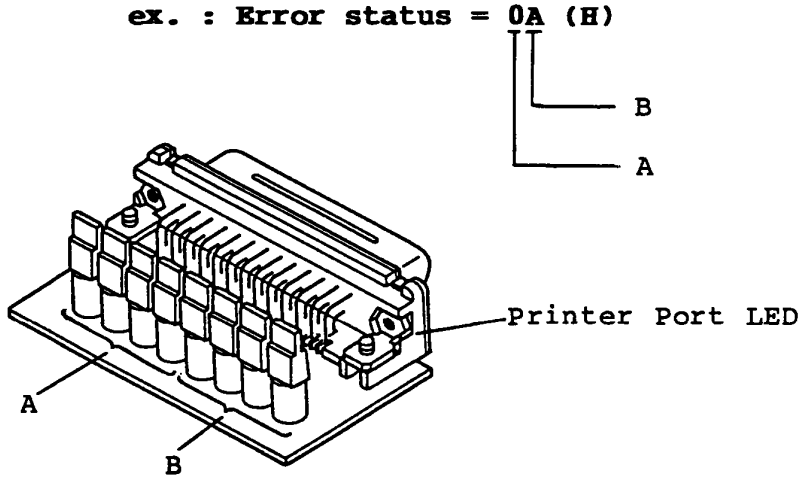


Figure 4-7 Indicat on the Printer Port LED

(order number :

3. In the following flow chart of the Power-On Diagnostics, sequence of the subtest executions is shown by arrow marks. In each subtest, all possible error status and information corresponding the error are described as below.

To be continued.

Read error status and isolate the failure component (continued)

Test Name	Status	
	OK	No good
CPU Test	AA (H)	
↓		
BIOS ROM Test	D5 (H)	01 (H)
↓		
Timer(82C53) Test	12 (H)	02 (H) 03 (H)
↓		
DMAC(82C37) Test	14 (H)	04 (H) 05 (H)
↓		
RAM R/W Test for First 16KB	16 (H)	06 (H) 07 (H)
↓		
PIC(82C59) Test	18 (H)	08 (H) 09 (H) 0A (H) 0B (H)
↓		
VIDEO RAM Test		0C (H)
↓		
DISPLAY QA Test	FE (H)	0D (H) 0E (H)

Is the Error Status disappear ?

Yes: Go to **SYSTEM PCB-1.**

No: Go to **SYSTEM PCB-4.**

POWER
(Power Supply Unit)

You have reached this TIP since the Power Supply Unit is suspected of the cause of failure.

You need to prepare the good Power Supply Parts and Power Supply Unit for maintenance.

The symptom may be one of follows.

1) No character is on the LCD Display.

2) No LED is on the Printer Port LED.

3) Power/Speed indicator could not be OFF.

4) Error status is disappeared on the Printer port LED.

Go to **POWER-1** for the symptom 1, 2, 3 or 4 of the above.

LED (Low Batt.) check

1. Turn ON the power switch of the System Unit.
2. Confirm that the LED (Low Batt.) of indicator lighting.

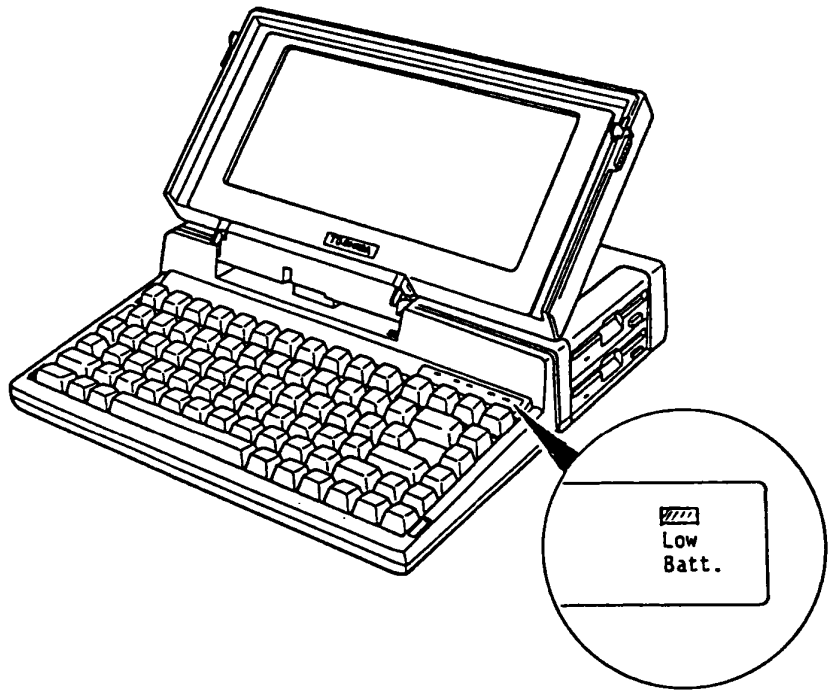


Figure 4-8 LED (Low Batt.) Check

Is the LED (Low Batt.) lighting ?

Yes: You need to charge the batteries, then repeat the operation.
If failure remains, go to **POWER-4.**

No: Go to **POWER-2.**

Connector Check

1. Turn OFF the power switch of the System Unit.
2. Disassemble the Upper Cover of the System Unit.
   (Refer to PART 5)
3. Check that the three cables (PJ1, PJ3, PJ4) are connected correctly & securely.

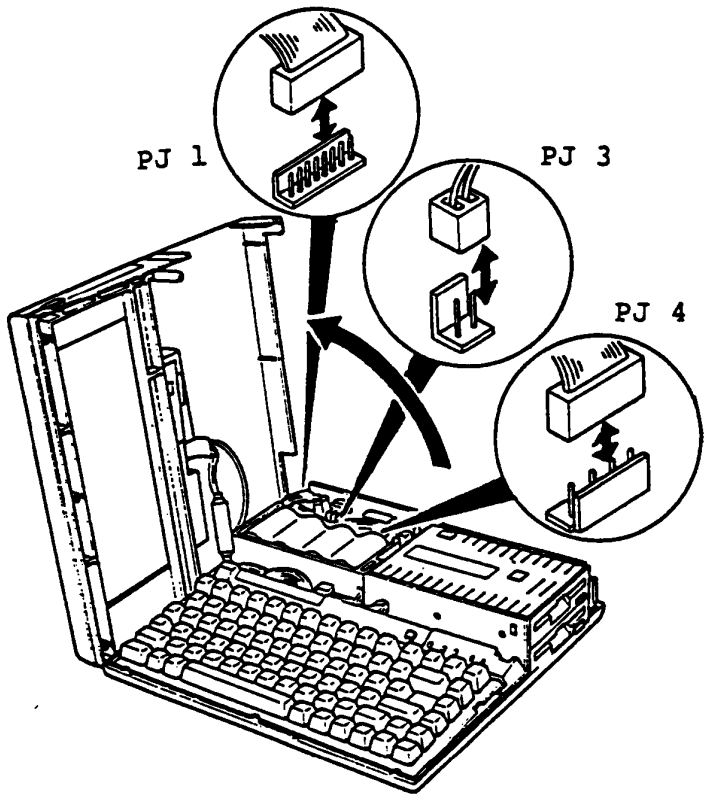


Figure 4-9 Connector Check

Are the connectors and cables connected correctly & securely ?

Yes: Go to **POWER-3.**

No: Correct them and repeat the operation to verify it. If failure remains, go to **POWER-3.**

Output voltage check

1. Turn ON the power switch of the System Unit.
2. Check all output voltage of +9V, -9V, -15V and +5V DC with AVO meter. (Refer to next page)

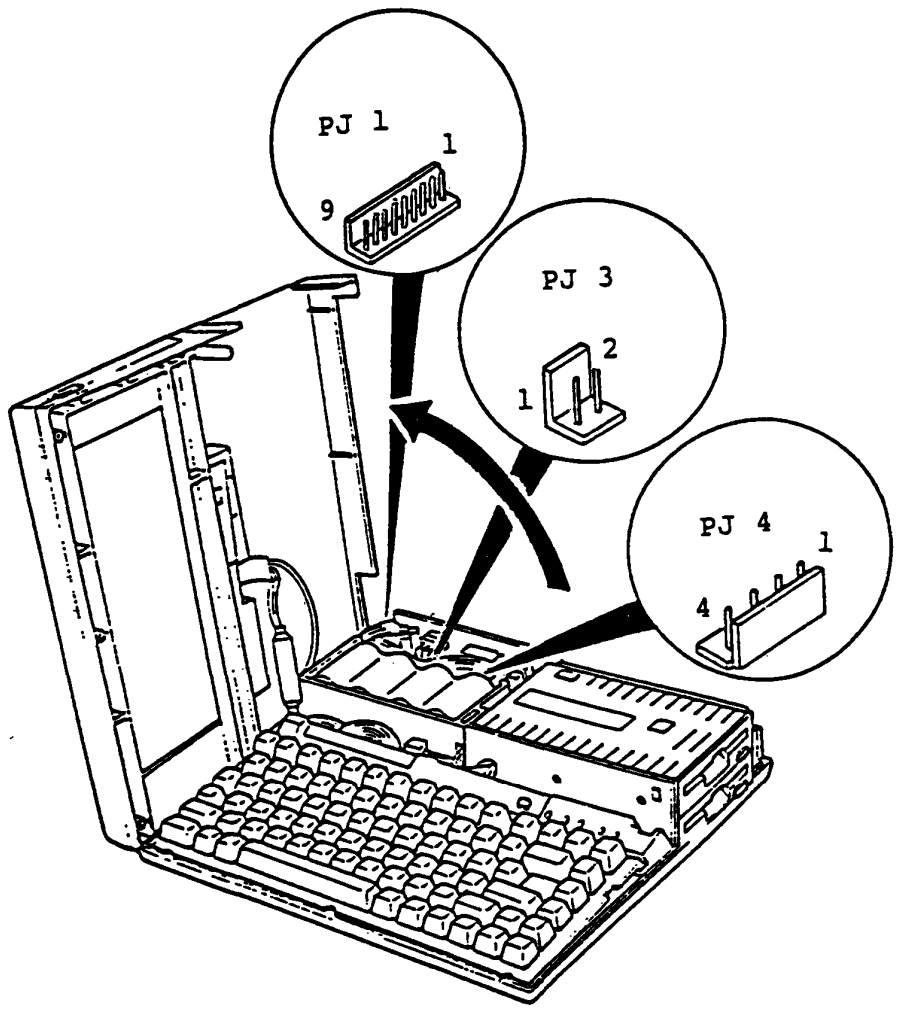


Figure 4-10 Output Voltage Check

To be continued.

Output voltage check (Continued)

Output voltage torerance

Connector	Pin		Voltage		
	+lead	-lead	Normal Vdc	Min Vdc	Max Vdc
PJ 1	1	4	+ 9	+7.7	+10.4
	2	4	- 9	-10.4	-7.7
	3	4	- 15	-15.8	-14.2
PJ 4	1, 2 ~~1~~	3, 4 ~~2, 4~~	+ 5 ~~+ 12~~	+4.8	+5.7
	~~3~~	~~2, 4~~	~~- 9~~		

Are all output voltages in tolerance ?

Yes: Power Supply PCB and Battery Package is good.

No: In the case of the PJ 3 output voltage in tolerance, go to **POWER-4.**
In the case of the PJ 1 and PJ 4 output voltage in tolerance, go to **POWER-5.**

Replacement Battery Package

1. Turn OFF the power switch of the Power Supply Unit.
2. Replace the suspected Battery Package with a good spare Battery Package.
3. Turn ON the power switch of the System Unit.
4. Repeat the operation to verify it.

Does the failure remain ?

Yes: Battery Package is good.
Go to **POWER-5.**
No: Battery Package is faulty.

Replacement Power Supply PCB

1. Turn OFF the power switch of the System Unit.
2. Replace the suspected Power Supply PCB with a good spare Power Supply PCB.
3. Turn ON the power switch of the System Unit.
4. Repeat the operation to verify it.

Does the failure remain ?

Yes: Power Supply PCB is good. Another Unit may be suspected.

No: Power Supply PCB is faulty.

You have reached this TIP since the System PCB is suspected of the cause of failure.
You need to prepare the Printer Port LED for maintenance and good spare System PCB for replacement.

The symptom may be one of follows.

1) The Power-On Diagnostics could not run at all.
   No error status is indicated on the Printer Port LED.

2) An error status has been indicated on the Printer Port LED during the Power-On Diagnostics.

Go to **SYSTEM-1** for the trouble shooting of above symptoms.

Set the Printer Port LED

1. Turn OFF the power switch of the System Unit.
2. Disconnect the all connectors from rear panel.
3. Connect the Printer Port LED (A) to the PRT/FDD connector (B) of the System Unit.
4. Confirm that PRT/FDD select switch (C) is set to PRT side.
5. Turn ON the power switch of the System Unit.
6. Check whether the symptom disappears or not to Printer Port LED.

(Refer to **POWER-ON DIAGNOSTIC**)

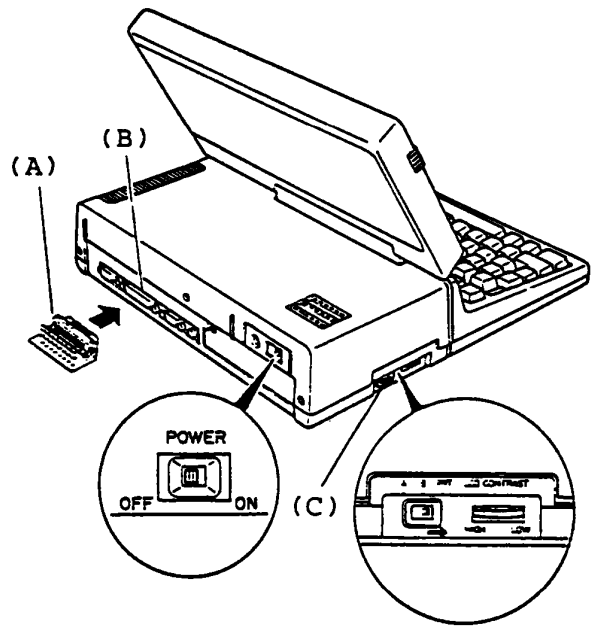


Figure 4-11 Set the Printer Port LED

Does the symptom disappear?

Yes: Failure is the one of separated units.
Connect each separated unit one by one to the System Unit and run Power-On Diagnostics for the failure unit isolation.
Turn OFF the power switch of the all units before making disconnection.

No: Go to **SYSTEM PCB-2.**

Remove all option PCB(s)

1. Turn OFF the power switch of the System Unit.

2. Remove all option PCB(s) (Expansion Memory Card (A) and Modem Card or Interface Card (B)).
   Note : If the mamory size of the System Unit have been changed you must change the setting of configuration DIP switch (C).

3. Turn ON the power switch of the System Unit then check the error status on the Printer Port LED.
   (Refer to **POWER-ON DIAGNOSTIC-3**)

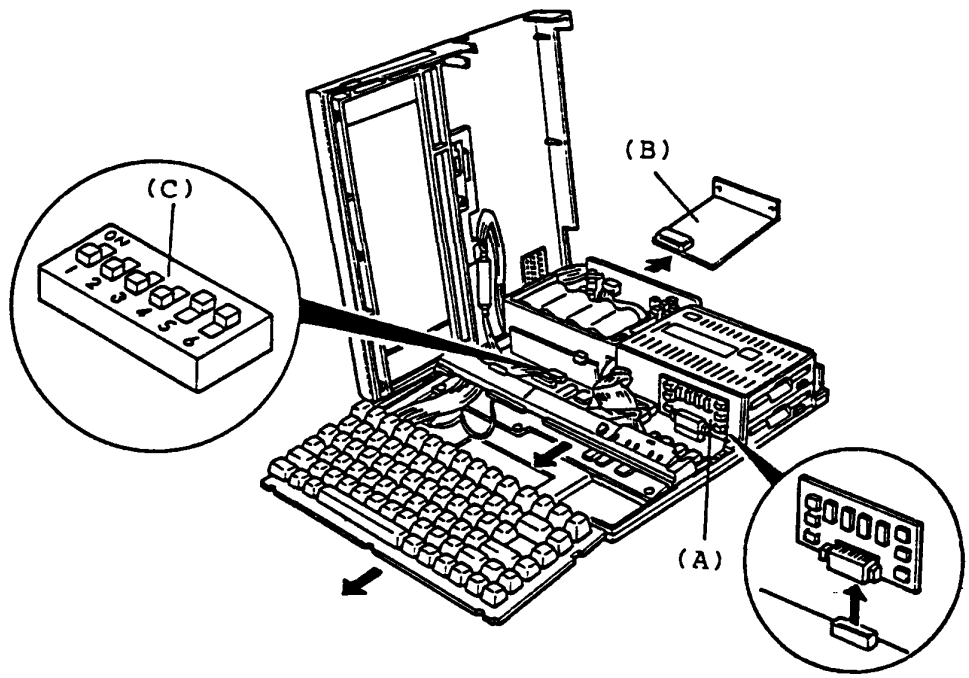


Figure 4-12 Option PCB Removal

Does the symptom disappear?

Yes: Failure is the one of option PCB(s).
Reinstall each option PCB one by one to the System Unit and run Power-On Diagnostics for the failure PCB isolation.
Turn OFF the power switch of the System Unit before making removal and reinstallation of each option PCB.

No: Go to **SYSTEM PCB-3.**

Disconnect all signal cables

1. Turn OFF the power switch of the System Unit.
2. Disconnect all signal cable connectors of Int. FDD (A), Indicator (B), LCD (C) and Keyboard Unit (D).
3. Turn ON the power switch of the System Unit, then check the error status on the Printer Port LED.

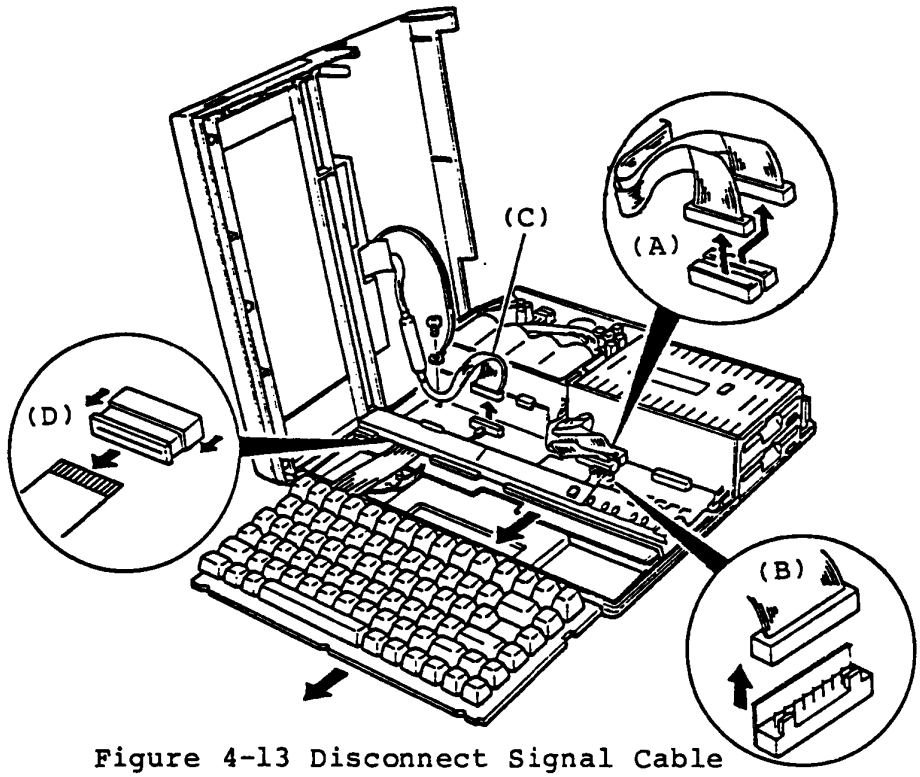


Figure 4-13 Disconnect Signal Cable

Does the symptom disappear?

Yes: Falure is one of Int. FDD, Indicator, LCD Display or Keyboard.
Connect each unit of them one by one to the System Unit and run Power-On Diagnostics for failure unit.
Turn OFF the power switch of the System Unit before each disconnection and connection of unit.

No: Go to **SYSTEM PCB-5.**

Voltage check

1. Check the voltages at connector pin with AVO meter.
   (Refer to next page.)
   Note: When you check the voltage at LCD connector (PJ2), connect the LCD connector to System PCB.
   GND point is (A).

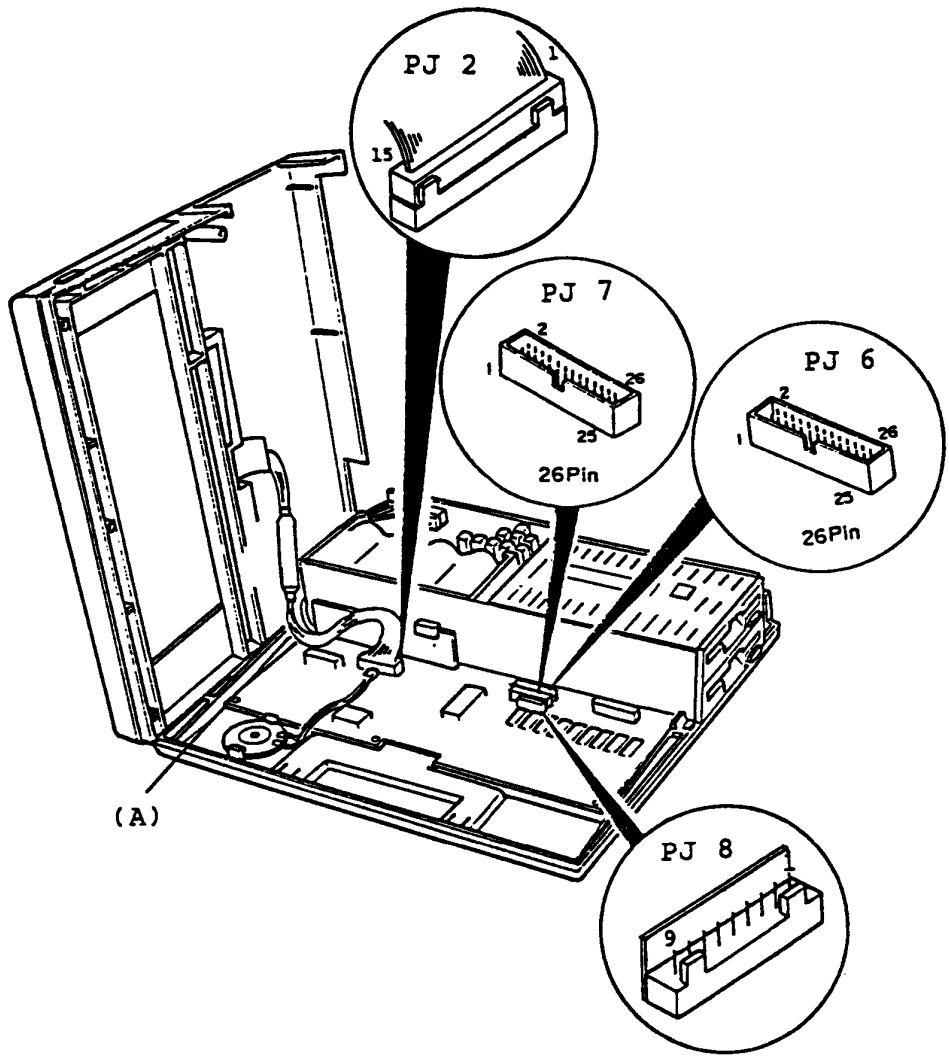


Figure 4-14 Voltage Check

To be continued.

Voltage check (Continued)

Voltage Tolerance

Connector	Pin		Voltage		
	+Lead	-Lead	Normal Vdc	Min Vdc	Max Vdc
PJ 2	12	GND	+ 5 (LCD)	+4.7	+5.6
PJ 6	1,3,5 7,9	GND	+ 5	+ ~~4.75~~ 4.8	+ ~~5.25~~ 5.7
PJ 7	1,3,5, 7,9	GND	+ 5	+ ~~4.75~~ 4.8	+ ~~5.25~~ 5.7
PJ 8	2	GND	+ 5	+4.8	+5.7
PJ 2	14	GND	-15	-15.8	-14.3

Is the voltage in tolerance?

Yes: Go to **SYSTEM PCB-6.**

No: Go to **POWER-1.**

System PCB replacement

1. Replace the suspected System PCB with a good spare System PCB.
   Note: You need to set the DIP switch. (Refer to page 1-10.)
2. Turn ON the power switch of the System Unit.
3. Repeat the operation to verify it.

Does the failure remain ?

Yes: The System PCB is good. Another Unit may be suspected.

No: The System PCB is faulty.

FDD
(3.5" Intarnal Floppy Disk Drive)

You have reached this TIP since FDD is suspected of the cause of the failure.
For the trouble shooting, you need to prepare one good spare 3.5" Int. FDD for the replacement.
You need to prepare one work disk for Test program and Cleaning disk for head cleaning. Work disk must be formated. (Refer to PART 8)

Before the trouble-shooting, confirm that PRT/FDD select switch of the T1100 PLUS System Unit is set to PRT position and rotate the LCD CONTRAST Dial fully to the direction of "High".

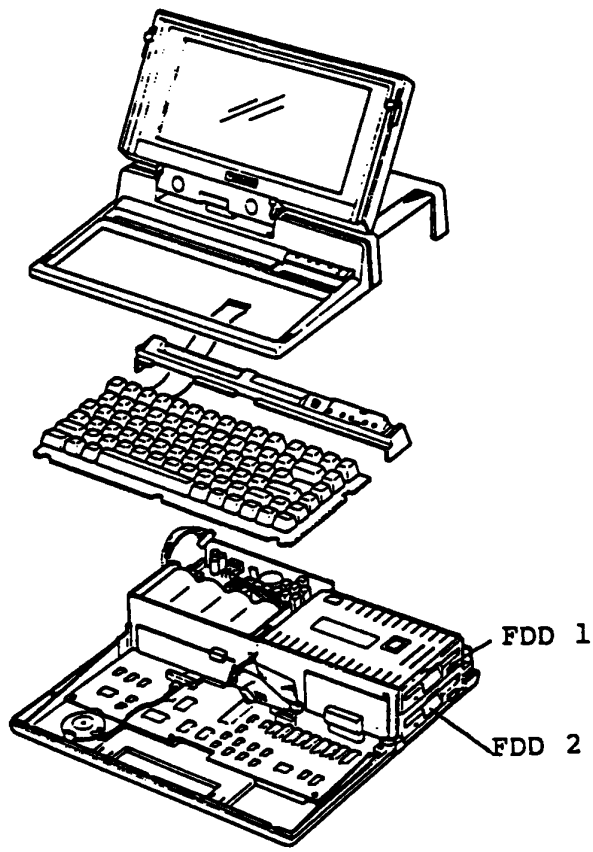
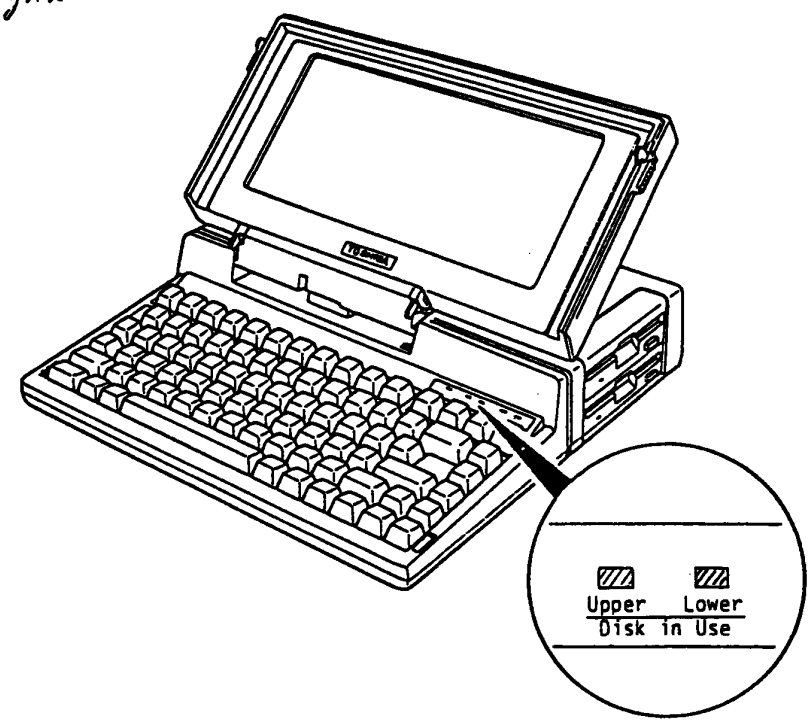


Figure 4-15 T1100 PLUS System Unit (F/F type)

LED of FDD Check

1. Confirm that the Floppy Disk is inserted into the FDD. If the Floppy Disk is inserted into the FDD, remove the Floppy Disk from the FDD.
2. Turn ON the power switch of the System Unit.
3. Confirme that both **Disk in Use** (Upper/Lower) indicators light sequentialy, ~~right~~ indicator (Upper) light at first, then ~~left~~ indicator (Lower) light.

right left



Figuren 4-16 LED Check

Is the LED lighting ?

Yes: Go to **FDD-2.**

No: System PCB may be faulty. Go to **SYSTEM-PCB**

The MS-DOS loading

1. Turn OFF the power switch of the System Unit.
2. Insert the MS-DOS system disk to the internal disk drive, then turn ON the power of the System Unit.
3. The MS-DOS is loaded after Power On Diagnostic execution.
4. After the MS-DOS loading, confirm that the following message appears on the display screen.
5. Press the "ENTER" key twice, then input file name of **CE Diagnostic** as **testce** to load the diagnostic program.

```
Toshiba  Personal Computer  (R2100EN)      Preliminary version

Copyright 1984,86 Toshiba Corporation

MS-DOS   Ver 2.11
Copyright 1983,84 Microsoft Corp.

Command  Ver 2.11V
Current date is  Wed  1-01-1986
Enter new date :
Current time is   0:36:46.00
Enter new time :

A>testce
```

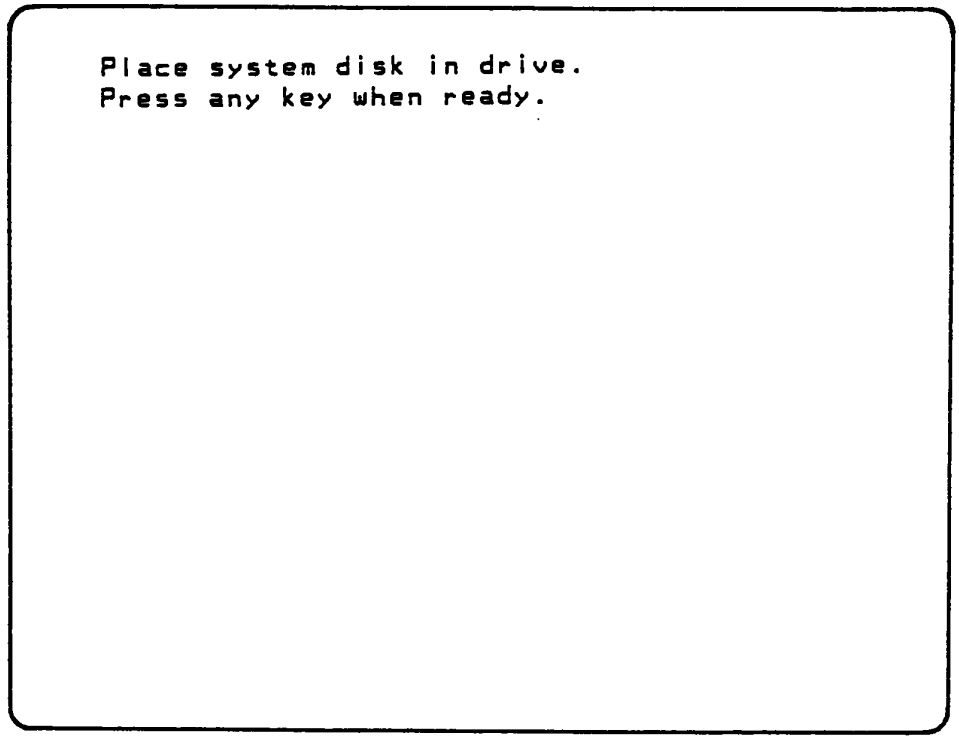
Is the above message displayed?

Yes: The underlined portion on the above screen are for the input **testce** message. Press the "ENTER" key.
Go to **FDD-5**.

No: Go to the next page.

Loading the MS-DOS (Continued)

6. Confirm that the following message on the display screen.



Does the above message appear ?

Yes: You may use a damaged system disk. Prepare the other good MS-DOS system disk, then repeat the turn ON the power switch of the System Unit to verify it.
Head of FDD may be dirty. Clean the head of FDD (Refer to **PART 8**).
If the failure remains, go to **FDD-10** (F type) or **FDD-4** (F/F type).

No: Go to **FDD-3.**

Prepare the good MS-DOS system disk

1. Turn OFF the power switch of the System Unit.
2. You may use a different system disk.
   Prepare the good MS-DOS system disk.
3. Turn ON the power switch of the System Unit.
4. Confirm that the MS-DOS is loarded. (Refer to **FDD-2**)

Is the MS-DOS loarded ?

Yes: Go to **FDD-5** .

No: Head of FDD may be dirty.
Clean the head of FDD (Refer to PART 8).
Repeat the opration to verify it, then if the MS-DOS is loaded, go to **FDD-10** (F Type) or go to **FDD-4** (F/F Type).

Use the FDD 2

1. Turn OFF the power switch of the System Unit.
2. Insert the MS-DOS system disk to other FDD (FDD 2).
3. Turn ON the power switch of the System Unit.
4. Confirm that the MS-DOS is loarded. (Refer to **FDD-2**)

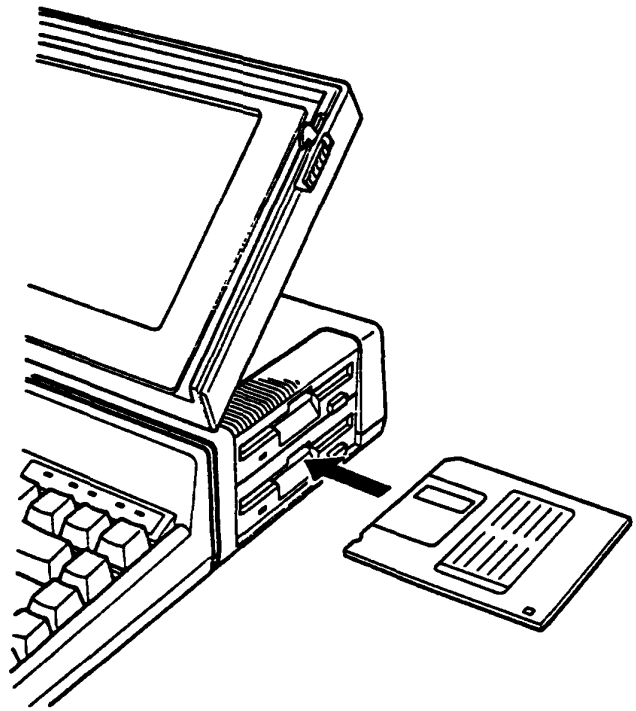


Figure 4-17 Use the FDD 2

Is the MS-DOS loaded ?

Yes: FDD 1 is faulty. Go to **FDD-10.**

No: Though FDD 2 is on ready, it may be interfered by FDD 1. Remove the Upper Cover (Refer to PART 5), disconnect the FDD 1 cable from System PCB.
Repeat the operation to verify, then the MS-DOS is loaded, go to **FDD-5.**
If the failure remains, go to **FDD-10.**

Diagnostic Menu Check

1. After the T&D program loading, confirm that the following Diagnostic Menu appears on the screen.

```
The TOSHIBA personal computer DIAGNOSTICS
version 0.12 (c) copyright TOSHIBA Corp 1986

DIAGNOSTICS MENU :

  1 - DIAGNOSTIC TEST
  2 - HARD DISK FORMAT
  3 - SEEK TO LANDING ZONE (HDD)
  4 - HEAD CLEANING
  5 - LOG UTILITIES
  6 - RUNNING  TEST
  7 - FDD UTILITIES
  8 - SYSTEM CONFIGURATION
  9 - EXIT TO MS-DOS




PRESS [1]-[9] KEY
```

Is the above message displayed?

Yes: Go to **FDD-6.**

No: You may use a damaged disk. Prepare the other MS-DOS system disk, then repeat the operation to verify it. (press "Ctrl"+"Alt"+"Del" keys)
If the failure remains, go to **FDD-10.**

Diagnostic Test Menu Check

1. Press "1" then "Enter" keys to display the Diagnostic Test Menu.

2. Confirm that the following Diagnostic Test Menu appears on the screen.

```
The TOSHIBA personal computer DIAGNOSTICS
version 0.12 (c) copyright TOSHIBA Corp 1986

DIAGNOSTIC TEST MENU :

   1 - SYSTEM TEST
   2 - MEMORY TEST
   3 - KEYBOARD TEST
   4 - DISPLAY TEST
   5 - FLOPPY DISK TEST
   6 - PRINTER TEST
   7 - ASYNC TEST
   8 - HARD DISK TEST
   9 - REAL TIMER TEST
  10 - NDP TEST
  88 - FDD & HDD ERROR RETRY COUNT SET
  99 - EXIT TO DIAGNOSTICS MENU



PRESS [0]-[9] KEY
```

Does the above message displayed?

Yes: Go to **FDD-7.**

No: You may use a damaged disk. Prepare the other MS-DOS system disk, then repeat the operation to verify it. (press "Ctrl"+"Alt"+"Del" keys)
If the failure remains, go to **FDD-10.**

Test Number Select

1. Press "5" then "Enter" keys to select the Floppy Disk Test.

2. Confirm that the following message appears under the Diagnostic Test Menu.

```
The TOSHIBA personal computer DIAGNOSTICS
version 0.12 (c) copyright TOSHIBA Corp 1986

DIAGNOSTIC TEST MENU :

   1 - SYSTEM TEST
   2 - MEMORY TEST
   3 - KEYBOARD TEST
   4 - DISPLAY TEST
   5 - FLOPPY DISK TEST
   6 - PRINTER TEST
   7 - ASYNC TEST
   8 - HARD DISK TEST
   9 - REAL TIMER TEST
  10 - NDP TEST
  88 - FDD & HDD ERROR RETRY COUNT SET
  99 - EXIT TO DIAGNOSTICS MENU

Test drive number select (1:FDD1,2:FDD2,0:FDD1&2) ?


PRESS [0]-[9] KEY 5
```

Does the above message appear ?

Yes: Select the test drive number.
For FDD 1 test, press "1" then "Enter" keys.
For FDD 2 test, press "2" then "Enter" keys.
For FDD 1 and FDD 2 test, press "0" then "Enter" keys.
Go to **FDD-8.**

No: You may use a damaged disk. Prepare other MS-DOS system disk, then repeat the operation to verity it.
(press "Ctrl"+"Alt"+"Del" keys)
If the failure remains, go to **FDD-10.**

Floppy Disk Test Menu

1. Confirm that the floppy Disk Test Menu is displayed as shown below.

```
FLOPPY DISK                              XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - Sequential read
02 - Sequential read/write
03 - Random address/data
04 - Write specified address
05 - Read specified address
99 - Exit to DIAGNOSTIC TEST MENU



SELECT SUB-TEST NUMBER  ?
```

2. Execute each sub-test in accordance with T&D operation procedures in PART 8.
   Note: You need to prepare the good Work Disk for test execution.

Is any error message display ?

Yes: Go to **FDD-9.**

No: FDD is good. Anoter Unit may be suspected.

Connector Check

1. Turn OFF the power switch of the System Unit.
2. Disassemble the Upper Cover. (Refer to PART 5)
3. Check that the FDD cable(s) (PJ 6, PJ 7) are connected correctly and securely.

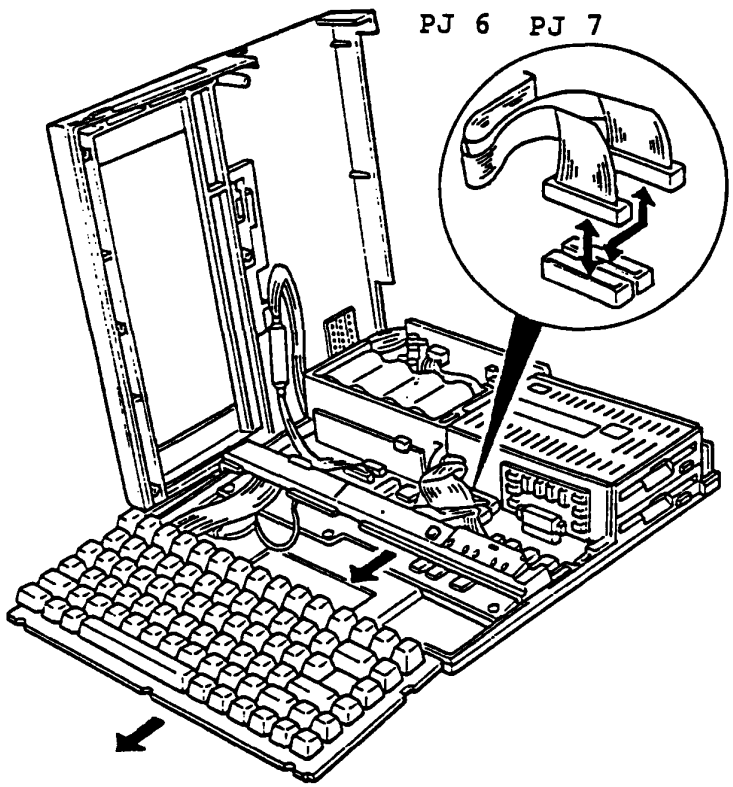


Figure 4-18 Connector Check

Is the FDD cable connection with the connector & correctly?

Yes: Go to **FDD-10.**

No Conneect them, then repeat the T&D operation to verify it.
If the failre remain, go to **FDD-10.**

FDD connector check

1. Turn OFF the power switch of the System Unit.
2. Remove the FDD Unit. (Refer to PART 5)
3. Spread the four nailes (A) with the blade screwdriver to remove as shown below.

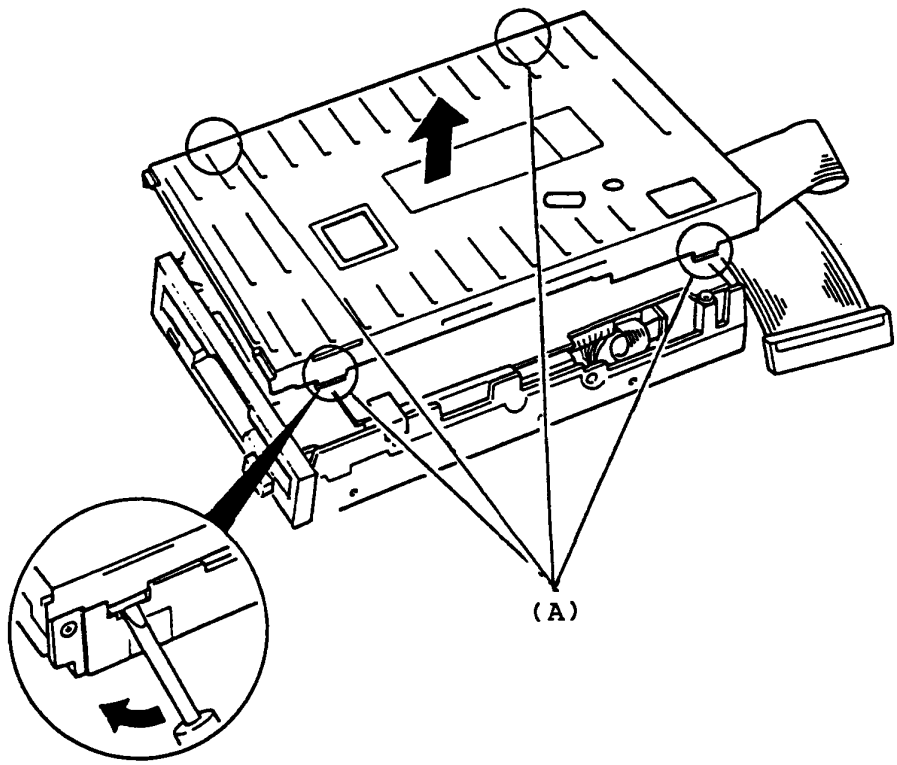


Figure 4-19 FDD Cover Removal

To be continued.

FDD conectors check (Continued)

4. Confirm that the five (J3, J4, J5, J6, J7) cables are connected to FDD PCB.

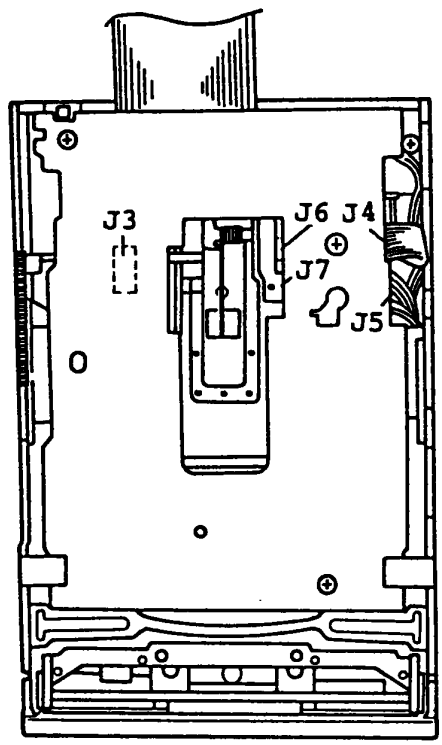


Figure 4-20 FDD PCB

Are the all cables connected ?

Yes: Go to **FDD-10.**

No: Connect them, then repeat the operation to verify it.

FDD PCB Replacement

1. Remove the two screws (A), then spread two nailes (B) with the blade screwdriver and disconnect the soket (C).

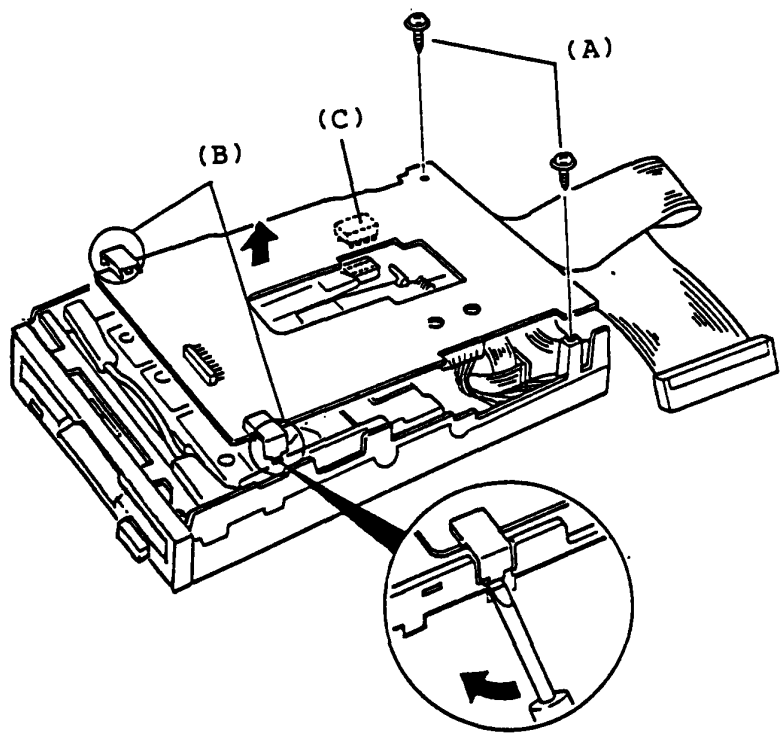


Figure 4-21 FDD PCB Removal

To be continued.

FDD PCB Replacement (Continued)

2. Disconnect two cables (D) from FDD PCB with a pair of tweezers hooking in the hole as shown below.
3. Disconnect the two connector (E) from the FDD PCB to remove.
4. Replace the suspected FDD PCB with a good spare FDD PCB.
5. Turn on the Power switch of the System Unit.
6. Repeat the T&D operation to verify it.

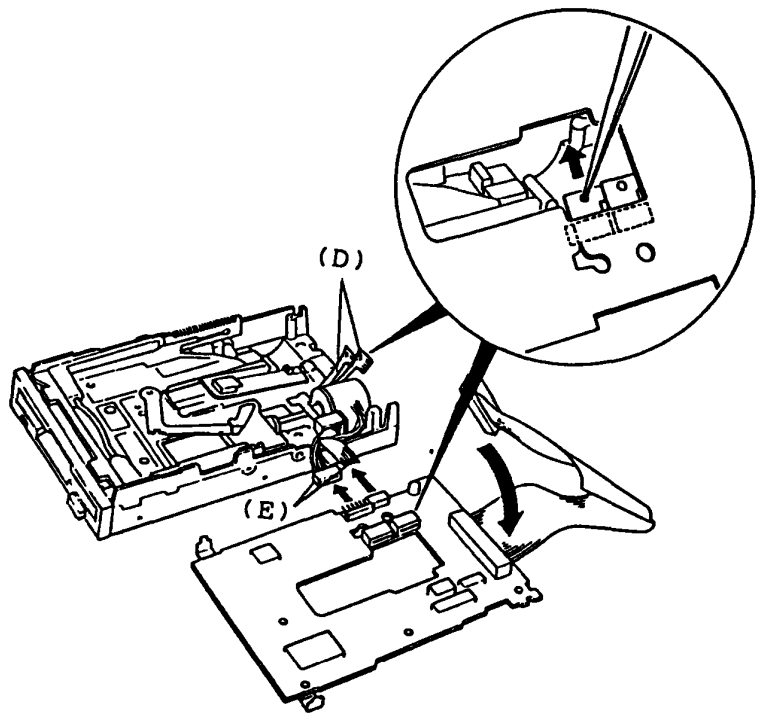


Figure 4-22 FDD PCB Removal

Does the failure remain ?

Yes: FDD PCB is good. Go to **FDD-12.**

No: FDD PCB is faulty.

FDD mechanical parts replacement

1. Replace the suspected FDD mechanical parts with a good spare FDD Device.
2. Install the FDD Unit, then turn ON the power switch of the System Unit.
3. Repeat the T&D operation to verify it.

Does the Failure remain ?

Yes: The FDD mechanical parts is good. Go to **FDD-13.**

No: The FDD mechanical parts faulty.

FDD Replacement

1. Replace the suspected FDD with a good spare FDD.
2. Install the FDD Unit, then turn ON the power switch of the System Unit.
3. Repeat the T&D opration to verify it.

Does the failure remain ?

Yes: The FDD is good. Another Unit may be suspected.

No: The FDD is faulty.

FDD Adjustment

NOTE ...Following items are not applzed to field maintenance.

This section provides adjustment procedure of FDD Unit and it includes the following.

1. Disk rotation period adjustment
2. Offtrack adjustment
3. Track 00 sensor position adjustment
4. Index timing adjustment

Note: Adjustment should be performed in the above order because the adjustments have an effect on the driver chracteristics.

Adjustment Tools

Adjustment Items / Required Tools	Disk rotation period adjustment	Offtrack adjustment position	Track 00 sensor adjustment	Index timing adjustment
Exerciser	○	○	○	○
Oscilloscope		○	○	○
CE Disk (Epson TC-301)		○	○	○
Normal Disk	○		○	
#1 Phillips screwdriver		○	○	○
#1 Flat screwdriver		○	○	○
Precision flat screwdriver	○			○
Torque screwdriver		○	○	○
Adhesive agent (LOCTITE #601)		○		

Positions and Functions of Test Points

Eight test points are provided on the SMD-280 main board unit for measuring the signal waveforms required for adjustment and inspection.

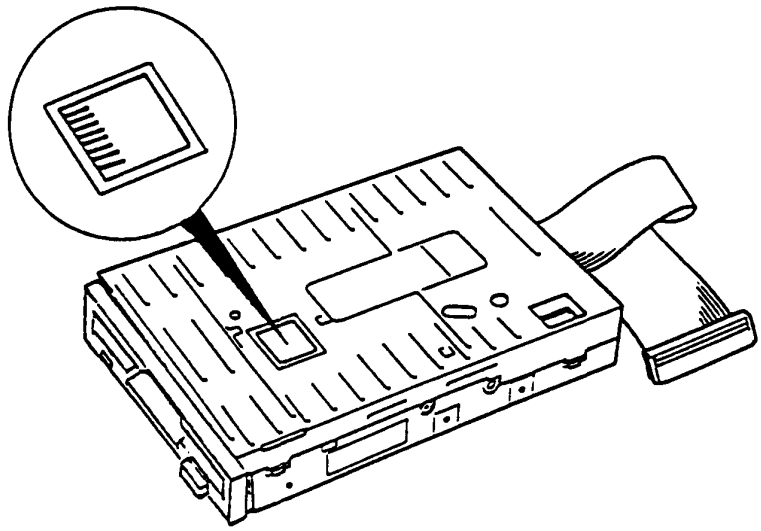


Figure 4-23 Position of Test Points

The contents of Test Pin as Follows.

TP-1(TKO) .... Test point for measuring the track 00 sensor position, the output level is Low and at track 1 or High at track 2.

TP-2(IDX) .... Test point for measuring the index signal.

TP-3(GND) .... An 0V (GND) analog signal line.
A reference point for measuring signal waveforms of TP-1, TP-2, TP-4, TP-5, TP-7, and TP-8.

TP-4(AMP) .... Test point for measuring read amplifiertput
TP-5(AMP) output. Differential waveforms which are 180 out of phase appear at TP-4 and TP-5.

TP-6(GND) .... 0V (GND) analog signal line.
A reference point for measuring the signal waveforms of TP-1, TP-2, TP-4, TP-5, TP-7, and TP-8.

TP-7(DIF) .... Test point for measuring differential
TP-8(DIF) amplfier output. Differential waveforms which are 180 out of phase appear at TP-7 and TP-8.

1. Disk rotation Period Adjustment

   Adjustment Procedure

   a) Turn off the power.
   b) Connect the cable of an exerciser to the connecter PJ
   c) Turn on the power of spindle moter.
   d) Set the normal disk.
   e) Seek the head to track 40.
   f) Adjust VR1 on the spindle motor unit and set the pulse interval of the index output as follows:
      200 ± 0.6sec

2. Offtrack Adjustment

Adjustment Procedure

a) Turn off the power.
b) Connect the SMD-280 to the Exerciser and connect TP-1 to CH 1 of the oscilloscope, TP-2 to CH2, and the Exerciser index output terminal to the external trigger.
c) Set the measuring conditions of the oscilloscope as follows:

Channel	CH1,CH2
AC-GND-DC	AC
VERT MODE	ADD
INVERT	ON
VOLTS/DIV	50 mV
TIME/DIV	20 msec

d) Turn on the spindle motor and set the CE disk.
e) Return the head to track 00. Next, move the head to track 40 using the STEP switch on the Exerciser.
f) Observe the offtrack signal waveforms on the oscilloscope. If the ratio between the right and left burst signal levels (small/large) is 0.8 or less, insert the Phillipes screwdriver into the screwdriver insertion holes on the main board unit and loosen the two stepping clamper mounting screws. Next, insert the stepping motor unit back and forth while turning the screwdriver. after adjusting the burst signal level ratio to 0.8 or more, tighten the stepping clamper mounting screws.
g) Apply the adhesive agent (LOCTITE #601) to the stepping clamper mounting screws.

3. Index Timing Adjustment

   Adjustment Procedure

   a) Turn off the power.
   b) Connect the SMD-280 to the Exerciser.
   c) Turn on the spindle motor and set the CE disk.
   d) Return the head to track 00. Next move the head to track 40 using the STEP switch on the Exerciser.
   e) Using the Exerciser, check that the index burst timing in the range 90-350 usec. If the timing in outside this range, adjust the index burst adjustment resistor (VR1).

4. Track 00 Sensor Position Adjustment

Adjustment Procedure

a) Turn off the power.
b) Connect the SMD-280 to the Exerciser.
c) Check that the offtrack adjustment has been completed by CE disk.
d) Set the measuring conditions of the oscilloscope as follows:

Channel	CH1
AC-GND-DC	DC
VERT-MODE	CH1
INVERT	-
VOLTS/DIV	1 V
TIME/DIV	0.1 msec

e) Connect TP-1 to CH1 of the oscilloscope and short the terminal 1 and 4 of J4 by wire.
f) Turn on the power.
g) Set the normal disk and turn on the Spindle motor. Move the head carrige unit to the outermost track.
h) Check whether the output at TP-1 is 1 V or less at track 2 using the oscilloscope.
i) Next, check whether the output at track 1.
j) Whn the outputs are more than 1 V at track 2 and less than 4 V at track 1, adjust them as follows.
k) Insert the Phllips screwdriver through the shield cover or main board unit and loosen the track 00 sensor mounting screw.
l) Next, insert the flat screwdriver btween the main frame groove and track 00 sensor mounting board.
m) While observing the oscilloscope, rotate the flat screwdriver and adjust the output at TP-1 until it is 1 V less at track 2 and 4 V or more at track 1.
n) Tighten the track 00 sensor mounting screw.

You have reached this TIP scince Keyboard is suspected of the cause of the failure.
You need to prepare good key-switch and key cap remover for remove the key switch for maintenance.
You need to prepare the good spare Keyboard Unit for replacement.

The symptom may be one of follows.

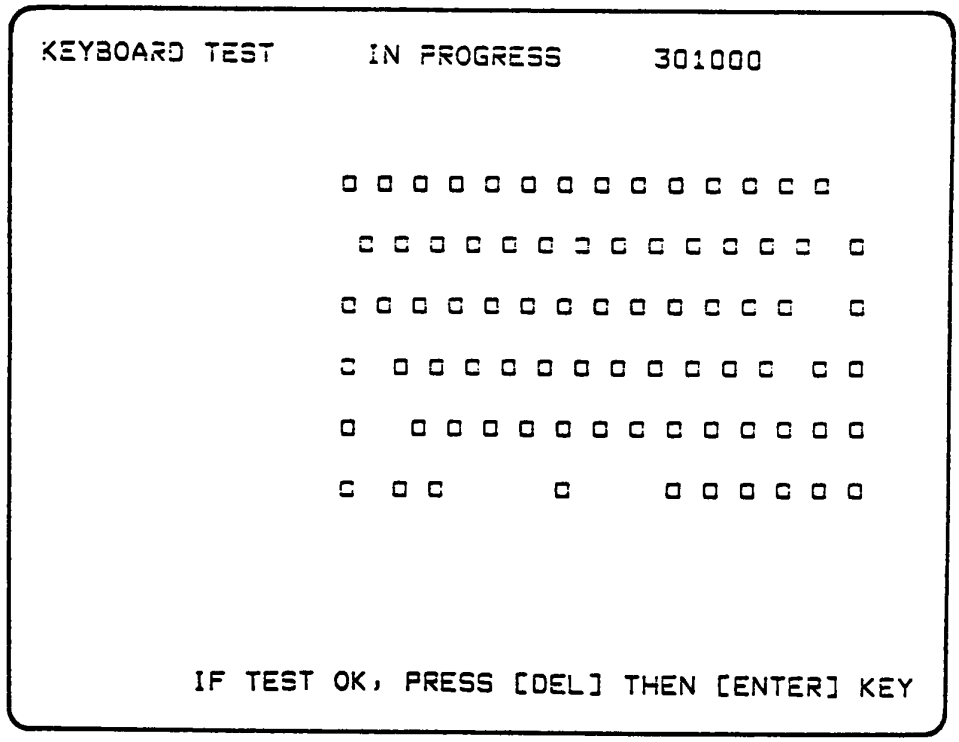
1. Character(s) are lost or changed incorrectly during key-in operation.

2. Excessive character(s) are transferred from the Keyboard to the System Unit.

Go to **KEYBOARD-1** for the symptom 1 and 2 of the above.

T&D Operation

1. Insert the MS-DOS system disk to the Int. FDD Unit of the System Unit.
2. Turn ON the power switch for the System Unit.
3. Execute the T&D program for keyboard in accordance with the T&D operation procedure of "PART 8".



Does all input operation function correctly ?

Yes: Another unit is suspected.

No: Go to next page.

T&D Operation (Continued)

The symptom may be one of follows.

1. All input operation do not function correctly:

   Go to **KEYBOARD-2.**

2. Specified input operation do not function correctly:

   Refer to Key Matrix and key number (See next page), then judge the Keyboard cable faulty or Key-switch faulty.
   If Keyboard cable faulty, go to **KEYBOARD-3.**
   If Key-switch faulty, go to **KEYBOARD-4.**

3. One or two input operation does not function correctly:

   The Key-switch may be faulty. Go to **KEYBORD-4.**

T&D Operation (Continued)

Table 4-1 Key Matrix

KBSCNb \ KBRTa	0	1	2	3	4	5	6	7
A	84							
9	14	80	71	28	41	54	55	82
8	13	72	26	27	77	40	53	58
7	11	12	25	75	38	39	52	83
6	9	10	23	24	36	37	51	50
5	7	8	21	22	35	48	49	57
4	5	6	19	20	33	34	47	46
3	3	4	17	18	31	32	44	45
2	1	2	15	16	30	29	42	43
1	60	70	62	73	64	66	68	56
0	59	69	61	81	63	65	67	79

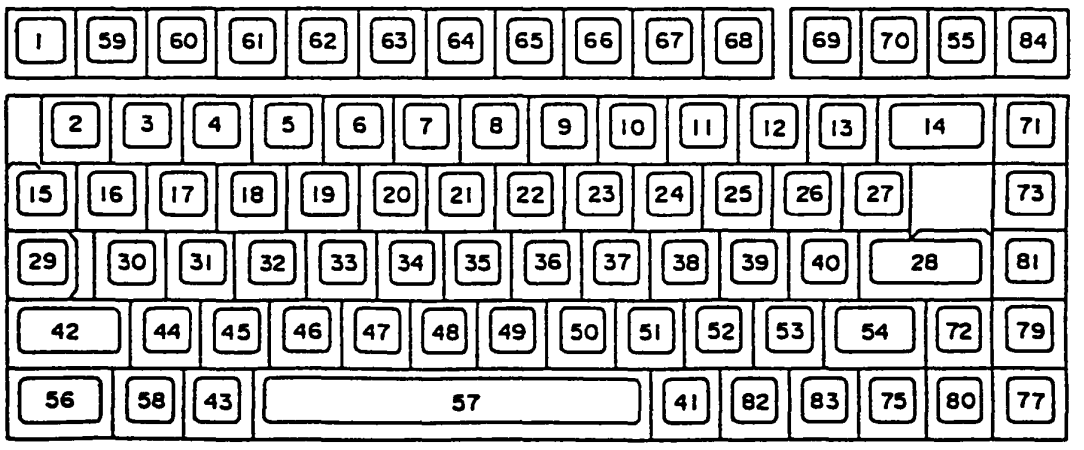


Figure 4-24 Key Number

Connector check

1. Turn OFF the power switch of the System Unit.
2. Disassemble the Upper Cover of the System Unit.
   (Refer to PART 5)
3. Check that the keyboard cable (A) connect on the System PCB.

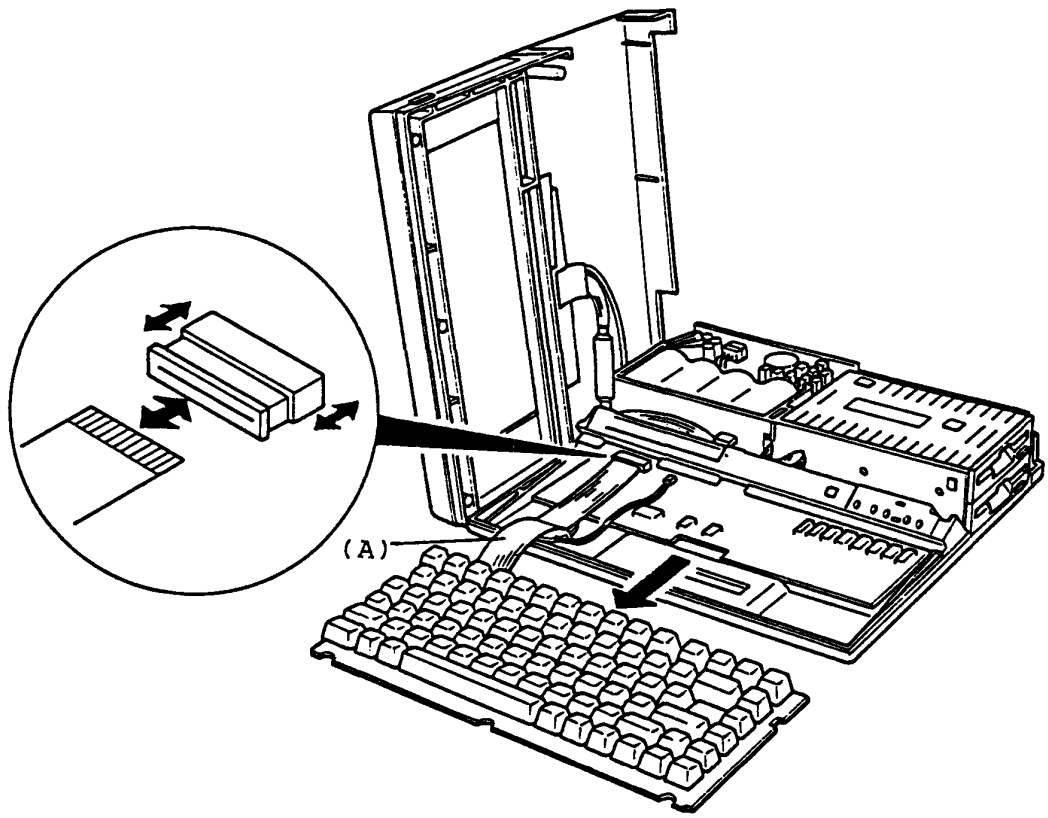


Figure 4-25 Connector check

Does the keyboard cable connect ?

Yes: Go to **KEYBOARD-3.**

No: Connect them, then repeat the operation to verify it.
If the failure remains, go to **KEYBOARD-3.**

Connector check for damage

1. Check the Keyboard cable for damage with AVO meter.

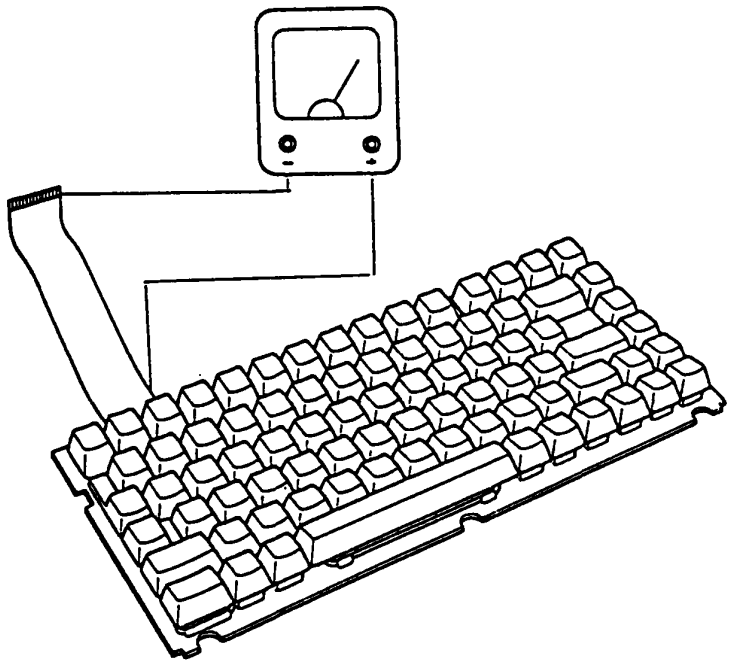


Figure 4-26 Check for Damage

Is there any damage on the Keyboard cable ?

Yes: Replace the Keyboard cable, then repeat the T&D opresion to verify it.
If the failure remains, go to **KEYBOARD-5.**

No: Go to **KEYBOARD-5.**

Key-switch replacement

1. Turn OFF the power switch of the System Unit.
2. Disassemble the Upper Cover of the System Unit.
   (Refer to PART 5)
3. Remove the Keyboard from the System Unit.
4. To replace a key cap, hold the cap with the attached key cap remover as in the bellow and pull it out right above.
   When fixing a key cap, push the key cap just a bit below.
5. Replace the Key-switch with good spare one.

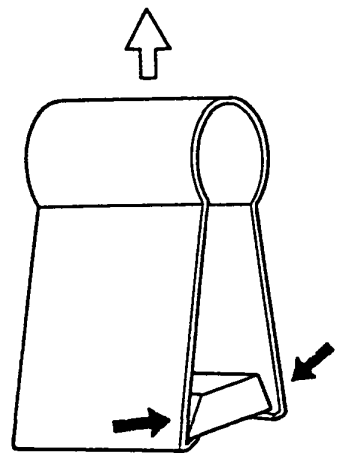


Figure 4-27 Key Cap Remover

Does the failure remain ?

Yes: Go to **KEYBORD-4.**

No: Key-switch is faulty.

Keyboard replacement

1. Replace the Keyboard and Keyboard Cable with good spare ones. (Refer to PART 5)
2. Turn ON the power switch of the System Unit.
3. Repeat the T&D operation to verify it.

Does the failure remain ?

Yes: The Keyboard is good. Another Unit may be suspected.

No: The Keyboard Unit is faulty.

You have reached this TIP since LCD Display is suspected of the cause of the failure.

The symptom may be one of the follows.

1. Neither of character nor graph appear on the LCD while the system is running.
2. Pictures on the LCD are distorted.

Go to **LCD-1** for the symptom 1 of the above.

Go to **LCD-15** for the symptom 2 of the above.

Display check

1. Turn ON the power switch of the System Unit.
2. Check that the display indicats all dots for a second momentarily.

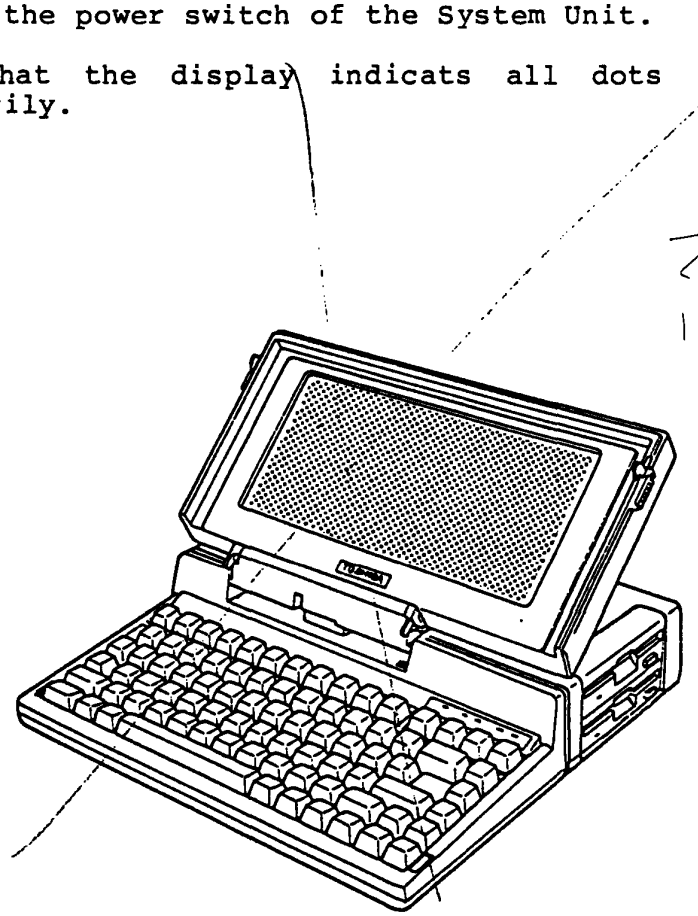


Figure 4-28 Display Check

Are the above all dots displayed ?

Yes: Go to **LCD-4.**

No: Go to **LCD-2.**

Upper/Lower half screen check

1. Check the LCD screen for whether a half of LCD screen is unable to display as shown in the figure 4-29.

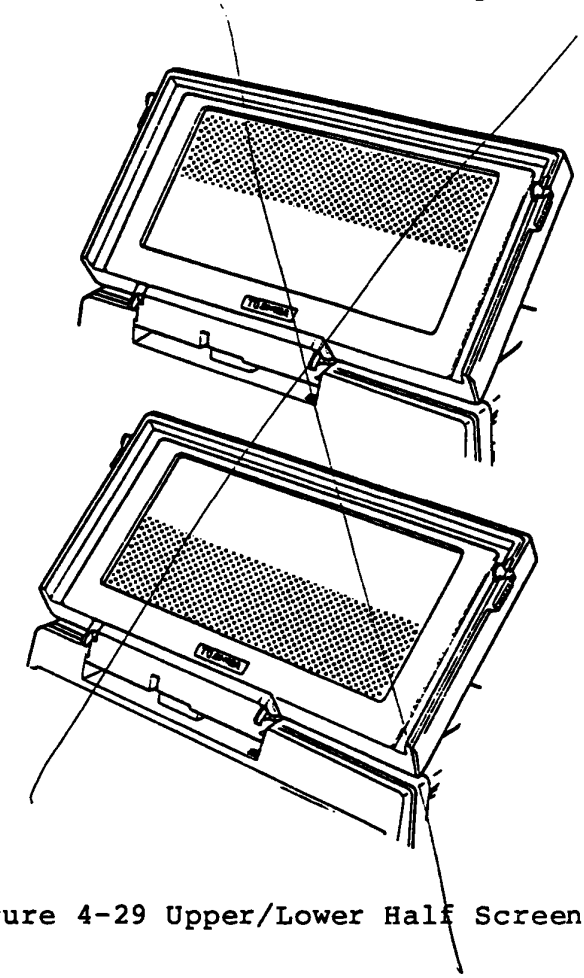


Figure 4-29 Upper/Lower Half Screen Check

Does above symptom appear ?

Yes: Go to **LCD-15.**

No: Go to **LCD-3.**

Extra dots or missing dots check

1. Check the extra dots and missing dots on a cetain column.

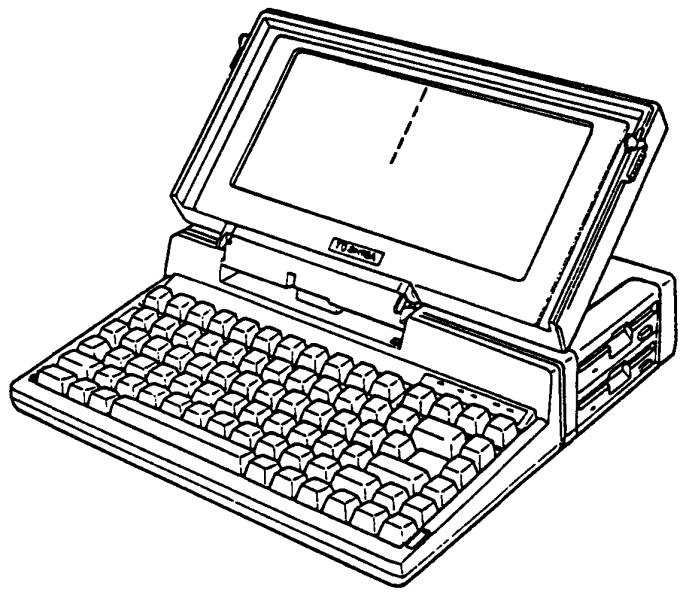


Figure 4-30 Extra Dots or Missing Dots Check

Are there any extra or missing dots ?

Yes: Go to **LCD-17.**

No: Go to **LCD-15.**

Screen check at the start up time

1. After the display indicats all dot, confirm that the following message appeared on the screen.

MEMORY TEST XXX KB

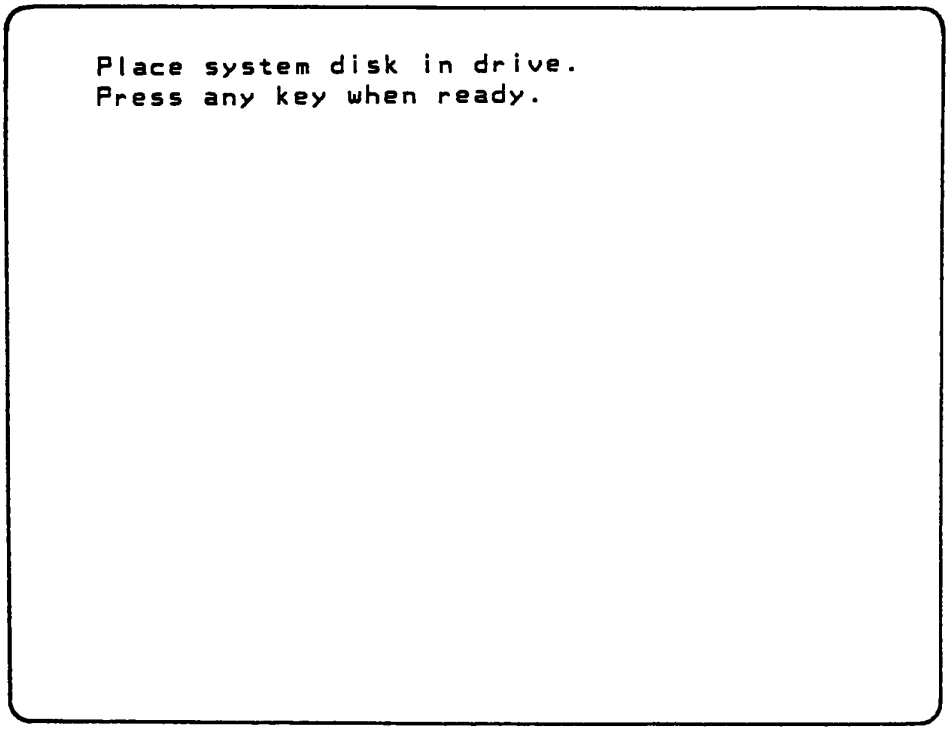
Does the above message appears ?

Yes: Go to **LCD-5.**

No: Go to **LCD-15.**

Message check

1. After **"MEMORY TEST XXX KB"** message appears on the screen, confirm that the following message appears on the screen.



Does the above message appear ?

Yes: Go to **LCD-6.**

No: Go to **LCD-15.**

Display Test Menu check

1. After the MS-DOS loading, run the Test & Diagnostic.
2. Press "4" then "Enter" keys for selecting the Display test of **DIAGNOSTIC TEST MENU.** (Refer to PART 8)
3. Confirm that the following Display Sub-test Menu appears on the screen.

```
DISPLAY TEST                              XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - VRAM read/write
02 - Character attributes
03 - Character set
04 - 80 * 25 Character display
05 - Graphics display (color set 0/1)
06 - 640 * 200 Graphics display
07 - 640 * 400 Graphics display
08 - Display page
09 - "H" pattern display
99 - Exit to DIAGNOSTIC TEST MENU


SELECT SUB-TEST NUMBER  ?
```

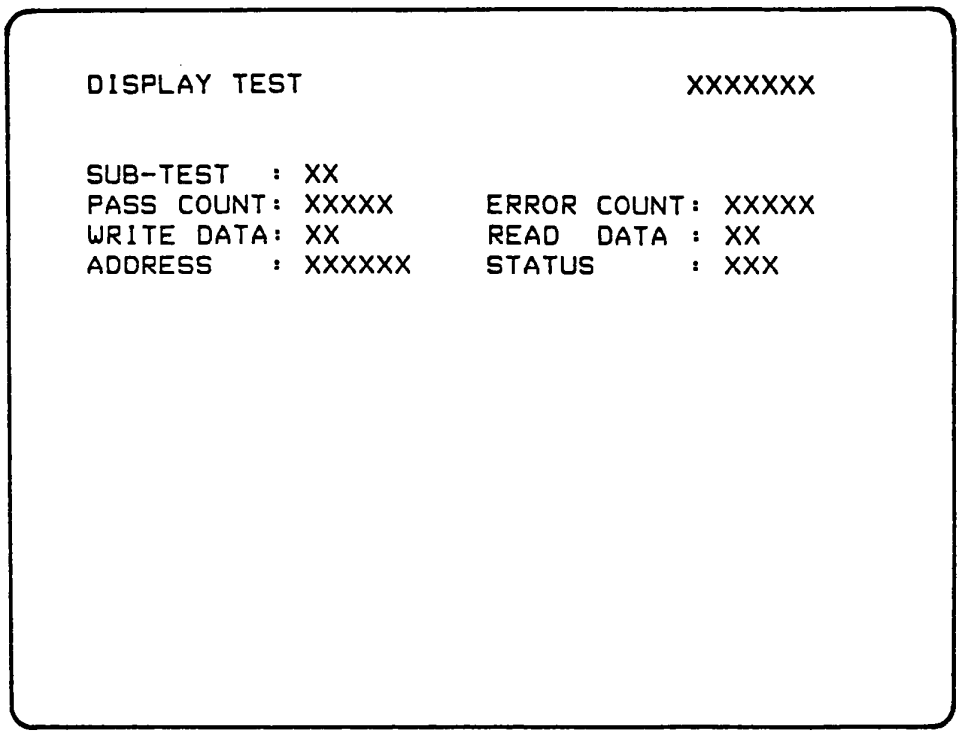
Does the above message appear ?

Yes: Go to **LCD-7.**

No: Go to **LCD-15.**

(01) VRAM read/write

1. Press **01** then keys on the Display test menu.
   The following message appears on the screen for very short time, then it returns to the Display Test Menu.



Does the error message appear ?

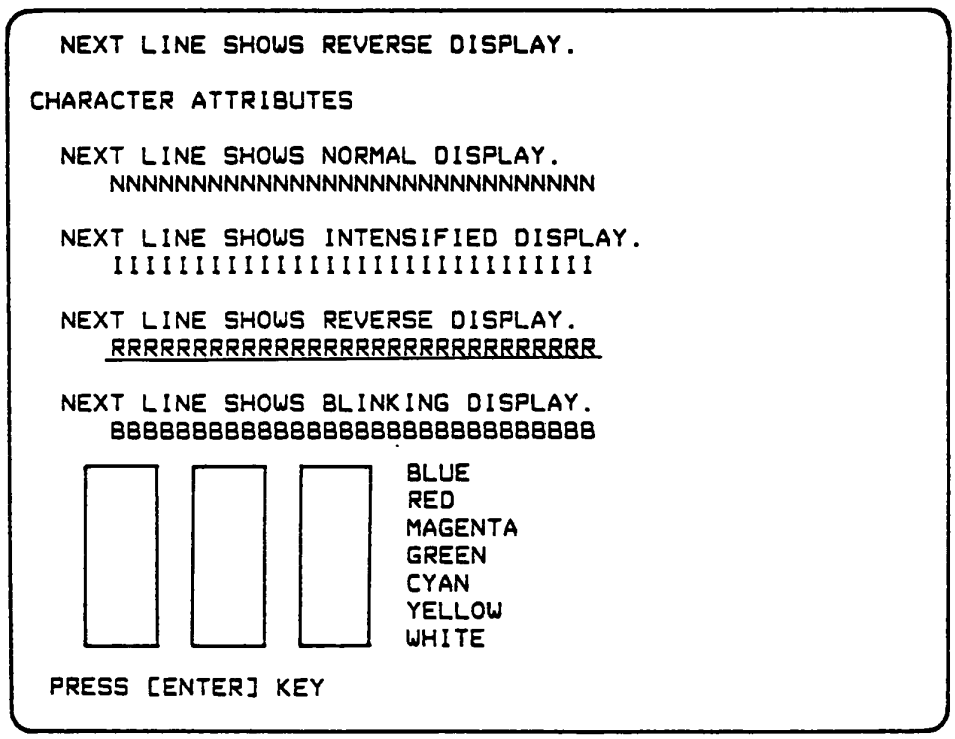
Yes: System PCB is faulty.
Replace the System PCB (Refer to PART 5), then repeat the T&D operation to verify it.

No: Go to **LCD-8.**

(02) Character attributes

1. Press 02 then **ENTER** keys while the Display Test Menu appears.
   The following pattern appears on the screen.
   Note: The underline position of following screen display , "**RRR.....**" to turn on and off.

2. Press **ENTER** key to return to the Display Test Menu.



Is the above pattern displayed correctly

Yes: Go to **LCD-9.**

No: System PCB is faulty.
Replace the System PCB (Refer to PART 5), then repeat the T&D operation to verify it.

(03) Character set

1. Press **03** then **ENTER** keys on the Display Test Menu, then the following pattern appears on the screen.
2. Press **ENTER** key to return to the Display Test Menu.

Is the above pattern displayed correctry ?

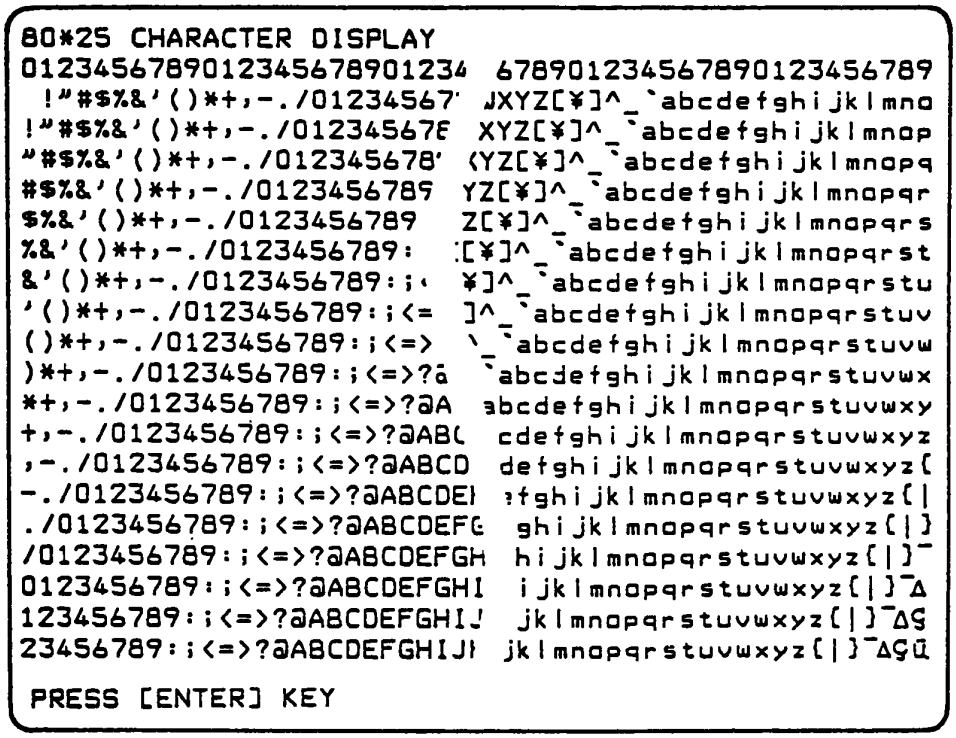
Yes: Go to **LCD-10.**

No: System PCB is faulty.
Replace the System PCB (Refer to PART 5), then repeat the T&D operation to verify it.

(04) 80 * 25 Character display

1. Press **04** then **ENTER** keys while the Display Test Menu appears.
   The following pattern appears on the screen.

2. Press **ENTER** key to return to the Display Test Menu.



Is the above pattern displayed correctly ?

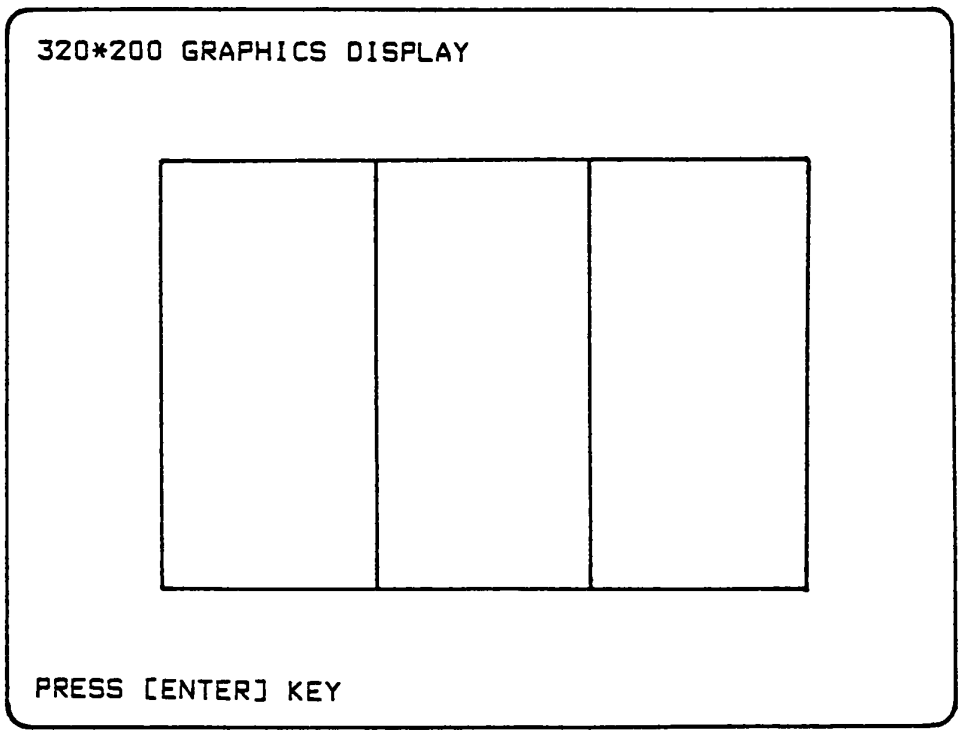
Yes: Go to **LCD-11.**

No: System PCB is faulty.
Replace the System PCB (Refer to PART 5), then repeat the T&D operation to verify it.

(05) Graphics display (color set 0/1)

1. Press **05** then **ENTER** keys while the Display Test Menu appears.
   The following pattern appears on the screen.
   Note: Right most block is the brightest.

2. Press **ENTER** key to return to the Display Test Menu.



Is the above pattern displayed correctly ?

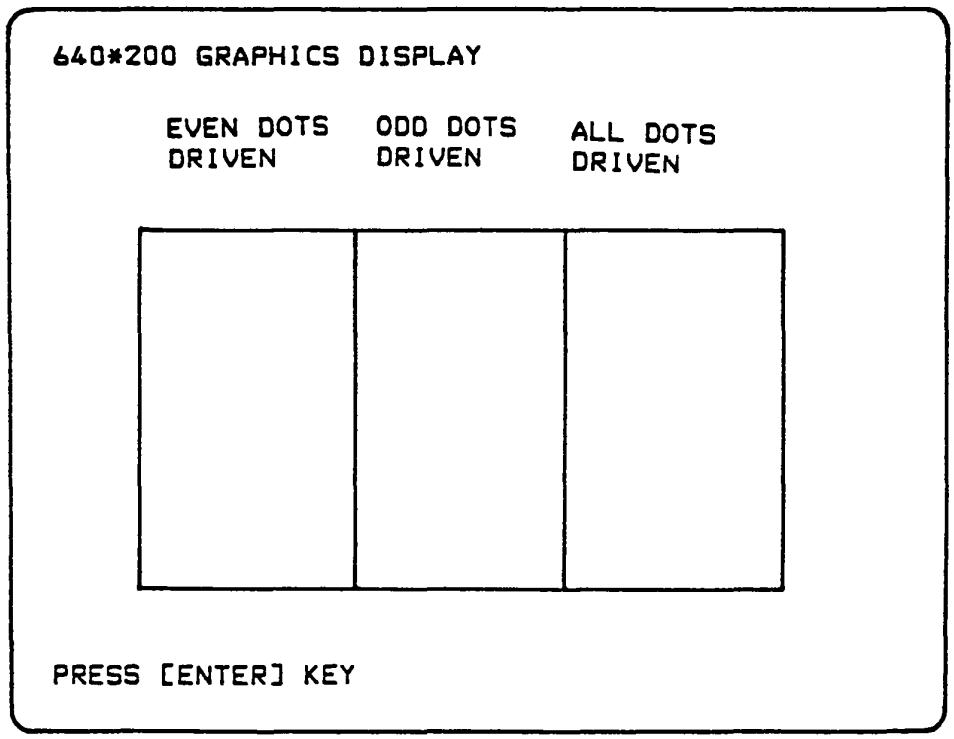
Yes: Go to **LCD-12.**

No: System PCB is faulty.
Replace the System PCB (Refer to PART 5), then repeat the T&D operation to verify it.

(06) 640 * 200 Graphics display

1. Press **06** then **ENTER** keys while the Display Test Menu appears.
   The following pattern appears on the screen.
   Note: Right most block (ALL DOTS DRIVEN) is the brightest.

2. Press **ENTER** key to return to the Display Test Menu.



Is the above pattern displayed correctly ?

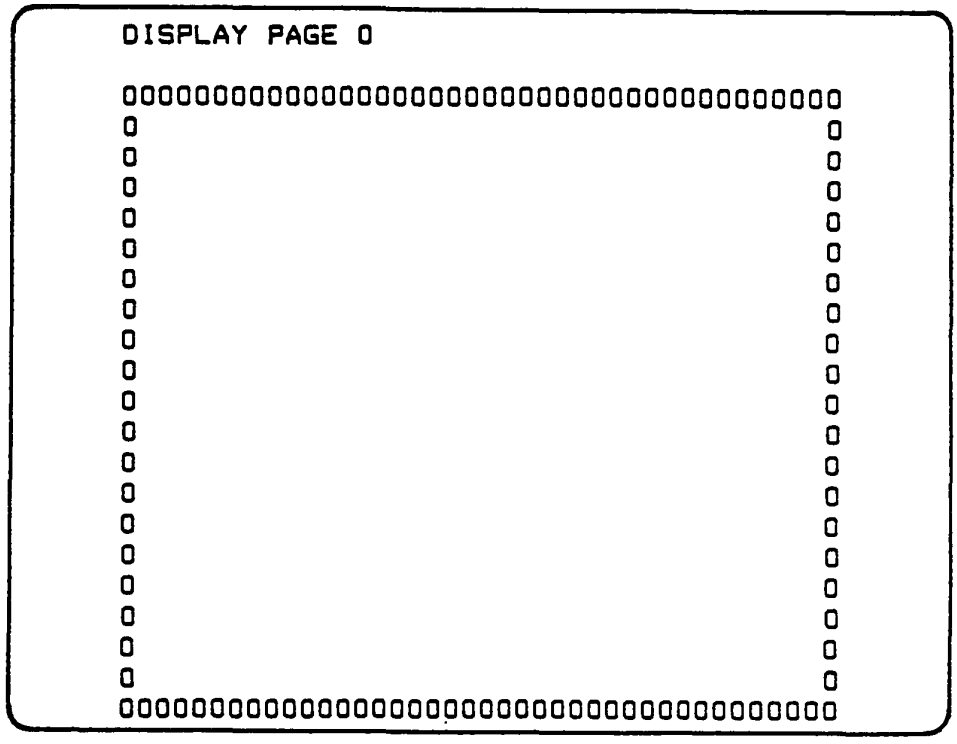
Yes: Go to **LCD-13.**

No: System PCB is faulty.
Replace the System PCB (Refer to PART 5), then repeat the T&D operation to verify it.

(08) Display page

1. Press **08** then **ENTER** keys while the Display Test Menu appears.
   The following patturn appears on the screen.
   Note: The following screen change a page number (0 - 7).

2. Press **ENTER** key to return to the Display Test Menu.



Is the above pattern displayed correctly ?

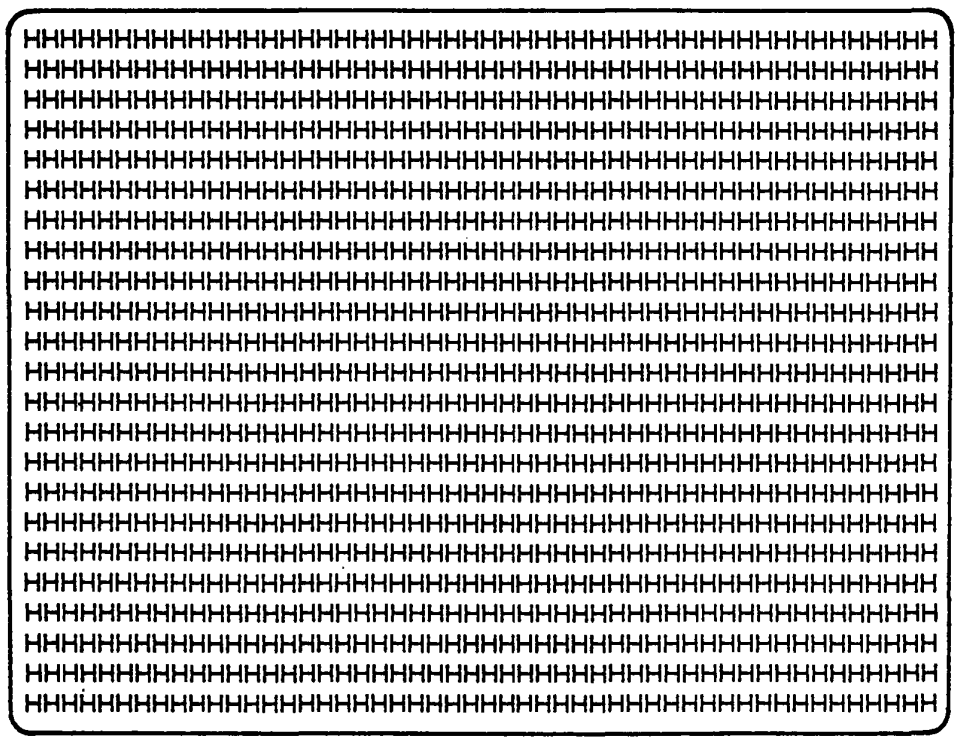
Yes: Go to **LCD-14.**

No: System PCB is faulty.
Replace the System PCB (Refer to PART 5), then repeat the T&D operation to verify it.

(09) "H" pattern display

1. Press **09** then **ENTER** keys while the Display Test Menu appears.
   The following pattern appears on the screen.

2. Press **ENTER** key to return to the Display Test Menu.



Is the above pattern displayed correctly ?

Yes: Go to **LCD-15**.

No: System PCB is faulty.
Replace the System PCB (Refer to PART 5), then repeat the T&D operation to verify it.

Connector Check

1. Turn OFF the power switch of the System Unit.
2. Remove the LCD from the LCD rear cover (Refer to PART 5), but the LCD cable.
   And put it on the Keyboard Unit.
3. Check the LCD connectors and cables are connected correctly & securely.

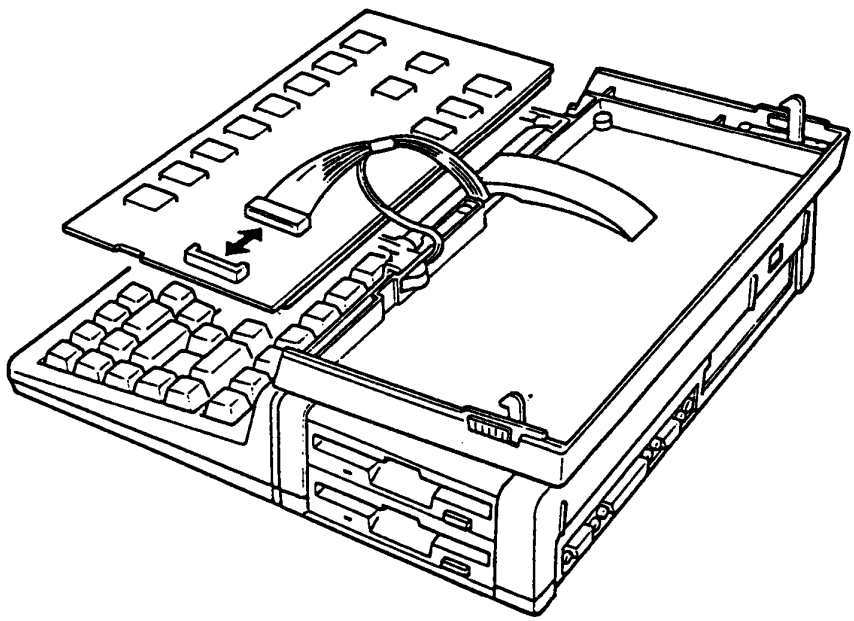


Figure 4-31 Connector Check

Are the connectors and cables connected correctly & securely ?

Yes: Go to **LCD-16.**

No: Connect it and repeat the T&D operation to verify it.

Voltage check

1. Check the Power voltage at the LCD connector for the appropriate voltage with AVO meter.

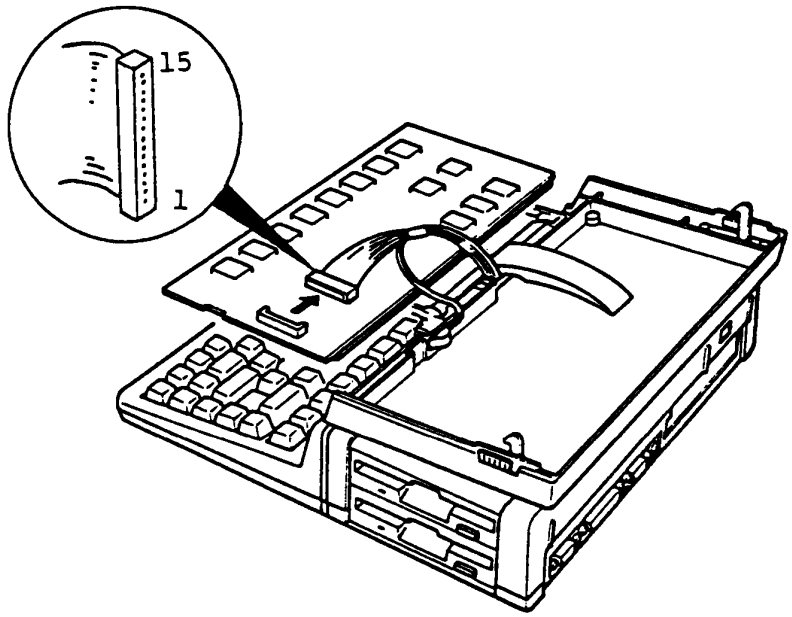


Figure 4-32 Voltage Check

Voltage Tolerance

Connector	Pin		Voltage		
	+ Lead	- Lead	Nomal Vdc	Min Vdc	Max Vdc
J 2	12	6,11,15	+ 5 (LCD)	+ ~~4.5~~ 4.7	+ ~~5.5~~ 5.6
	14	6,11,15	- 15	- ~~15.5~~ -15.8	- ~~14.5~~ -14.3

Are the voltages in tolerance ?

Yes: Go to **LCD-17.**

No: Go to **POWER.**

LCD Replacement

1. Turn OFF the power switch of the System Unit.
2. Replace the suspected LCD with a good spare LCD.
3. Turn ON the power switch of the System Unit.
4. Repeat the T&D operation to verify it.

Does the failure remain ?

Yes: The LCD is good. Another Unit may be suspected.

No: The LCD is faulty.

Ext. FDD
(5.25" External Floppy Disk Drive)

You have reached this TIP since Ext. FDD (External FDD) is suspected of the cause of the failure.
For the trouble shooting, you will need one good spare 5.25" Ext. FDD for the replacement.

External FDD is composed of following components.
You will isolate the faulty component from them in this TIP.

External FDD components

* FDD assembly
* FDD PCB (FDD5C1)
* Ni-Cd Battery Unit
* AC Adaptor
* Ext. FDD Cable

You need to prepair the following tools for this TIP.

Tools

* AVO meter
* MS-DOS System Disk (including T&D program file)
* Work Disk (formatted)
* Spair Ext. FDD Unit and Ext. FDD Cable
* Cleaning Disk (5.25")
* Screwdriver (phillips screwdriver)

Start from **Ext. FDD-1** for any trouble-shooting of Ext. FDD.

Set up for the FDD test

1. Connect the Ext. FDD cable to the T1100 PLUS System and the Ext. FDD.
2. Connect the AC adaptor to the Ext. FDD, and plug in AC plug of the AC adaptor to a wall-outlet.
3. Set the PRT/FDD select switch of the T1100 PLUS System to PRT position.
4. Insert the MS-DOS disk (including T&D program file) to the Int. FDD of the T1100 PLUS System.
5. Turn ON the power switches of the T1100 PLUS System and the Ext. FDD, then run the FDD test program according to the operation procedure of T&D (PART 8: TEST & DIAGNOSTICS).

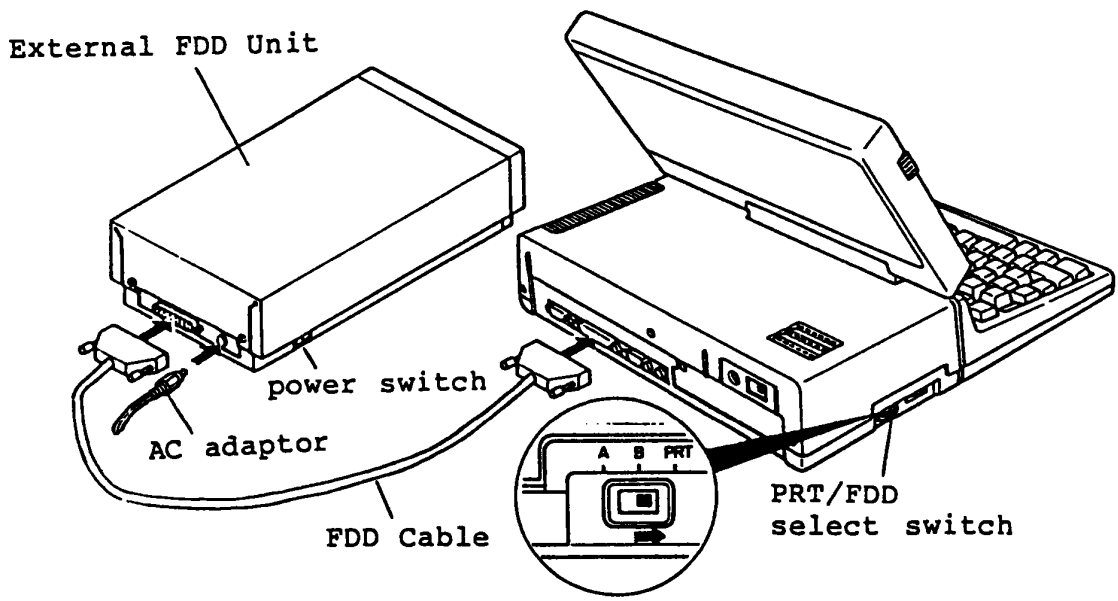


Figure 4-33 Set the External FDD

Go to **Ext. FDD-2.**

FDD test menu

1. Proceed the T&D program to FDD test menu (FDD test menu is as follow).

2. Set the PRT/FDD select switch of the System Unit to "A" position.

3. Insert the good 5-inch work disk (error free) into the Ext. FDD.

4. Run all subtests of the FDD test program according to the T&D program operation procrdure. (refer to PART 8: TEST & DIAGNOSTICS)
   Following figure is an example screen of FDD Test program.

```
FLOPPY DISK                              501000


SUB-TEST   : 01
PASS COUNT: 00000      ERROR COUNT: 00000
WRITE DATA: 00         READ  DATA : 00
ADDRESS    : 000000    STATUS     : 000

SUB-TEST MENU :

01 - Sequential read
02 - Sequential read/write
03 - Random address/data
04 - Write specified address
05 - Read specified address
99 - Exit to DIAGNOSTIC TEST MENU



SELECT SUB-TEST NUMBER  ? 01
TEST  LOOP (1:YES/2:NO) ? 2
ERROR STOP (1:YES/2:NO) ? 1
```

Does any error message apperar?

Yes: Clean the Read/Write head of the Ext. FDD with cleaning disk. For head cleaning, insert a cleaning disk to the Ext. FDD then select "HEAD CLEANING" on a DIAGNOSTIC MENU of T&D program. (refer to PART 8: TEST & DIAGNOSTICS)
If it leads you here again, go to **Ext. FDD-3** .

No: The Ext. FDD is good.

Voltage check

Check the voltages of the Ext. FDD as following.

1. Turn OFF the power switches of the T1100 PLUS System Unit and Ext. FDD.

2. Open the upper cover of the Ext. FDD. (Refer to PART 5: REPLACEMENT/ADJUSTMENT)

3. Turn ON the power switch of the Ext. FDD, then check the voltages for the FDD assembly by a AVO meter.
(All check points are shown in the Tables on next page.)

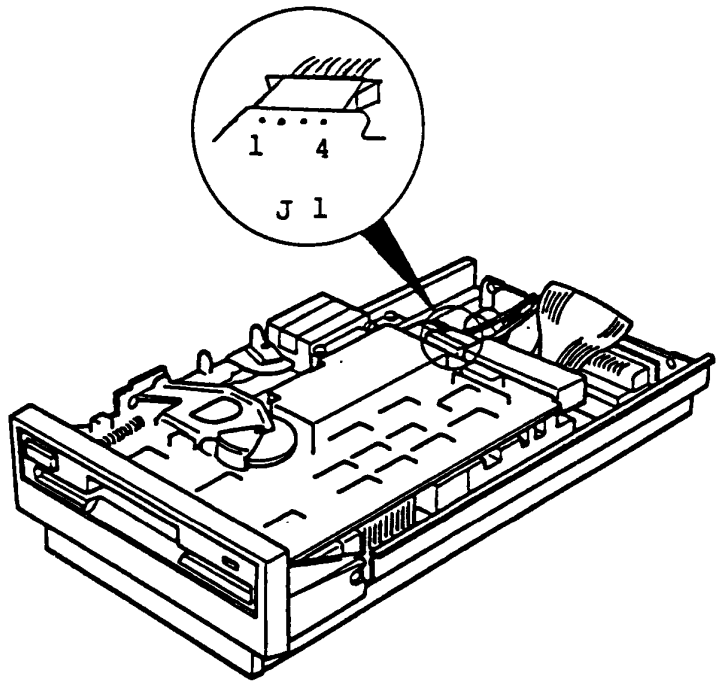


Figure 4-34 Voltage Check

To be continued.

Voltage check (continued)

Voltage Tolerances

Connector	Pin		Voltage		
	+Lead	-Lead	Normal Vdc	Min Vdc	Max Vdc
J1	1	2,3	+12	+11.5	+14.5
	4		5	+ 4.5	+ 5.3

Are the voltages within the torelance.

Yes: Go to **Ext. FDD-5**

No: Go to **Ext. FDD-4.**

Voltage check

If the voltages to FDD assembly are not in tolerance, one of the AC adaptor, FDD PCB or Ni-Cd battery is suspected.
Check all of them by a AVO meter as follows.

Note: Ni-Cd batter must be charged at least for an hour before the check.

1. Turn OFF the power switch of the Ext. FDD then pull out the DC plug of the AC adaptor from the Ext. FDD.

2. Check the voltage at the battery connector on the FDD PCB. (All check points are shown in the tables on next page.)

3. Check the output voltage of the AC adaptor at DC plug.

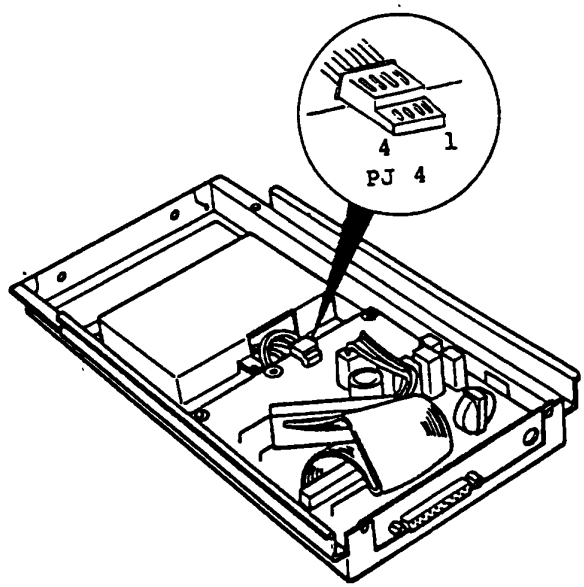
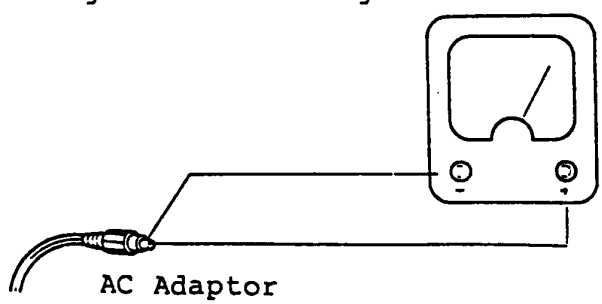


Figure 4-35 Voltage Check



AC Adaptor

Figure 4-36 AC Adaptor

To be continued.

Voltage check (continued)

Voltage Tolerances

Output of Ni-Cd Battery

Connector	Pin		Voltage
	+Lead	-Lead	
PJ4	1,2	3,4	More than 12 Vdc

Output of AC adaptor

Pin		Voltage		
+Lead	-lead	Normal Vdc	Min Vdc	Max Vdc
Inner Contact	Outer Contact	+20	+18	+22

If output voltage of Ni-Cd battery is out of tolerance:
===> Change the battery.

If output voltage of AC adaptor is out of tolerance:
===> Change the AC adaptor.

If both output voltages of the battery & the AC adaptor are in the tolerance:
===> Change the FDD PCB.

Connector & jumper strap check

1. Check all connectors of the suspected FDD assembly whether they are connected properly and securely.
2. Check the jumper strap settings on the FDD assembly PCB.

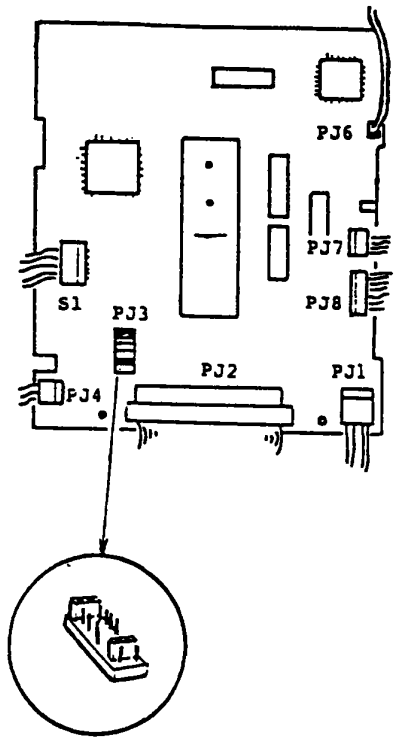


Figure 4-37 Jumper of FDD PCB

Are the connectors and jumper straps set properly?

Yes: Go to **Ext. FDD-6.**

No: Set the connector or the jumper strap properly then repeat to run FDD test program to verify it.
If it leads you here again, go to **Ext. FDD-6.**

FDD change

1. Turn OFF the power switches of the Ext. FDD & the T1100 PLUS System Unit.
2. Change the FDD assembly with a good one for checking.
3. Run FDD test program for the Ext. FDD.
   If an error occurs again, the FDD PCB (FFD5C1) or Ext. FDD cable are suspected.

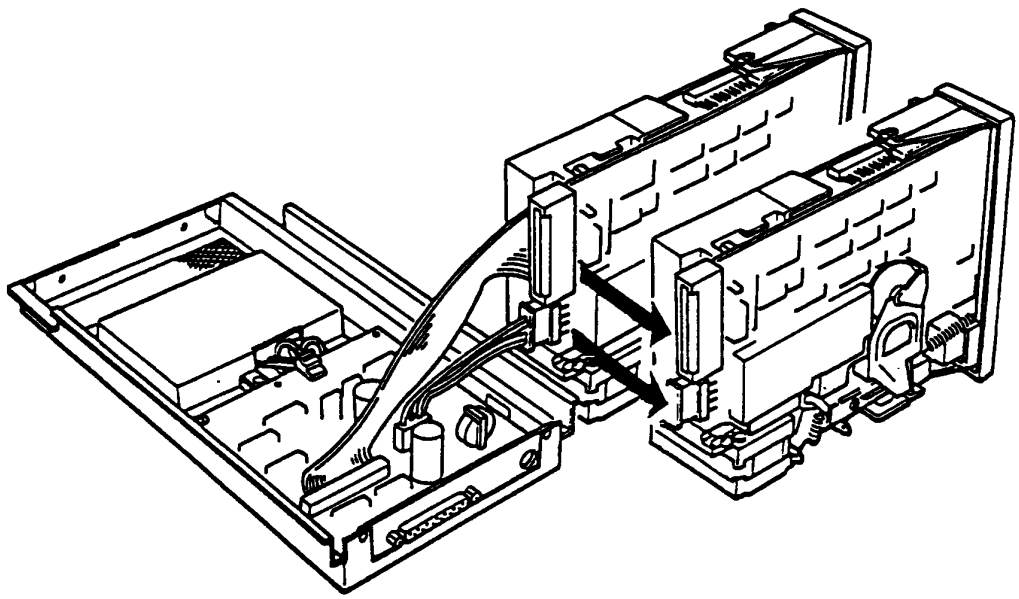


Figure 4-38 FDD Change

Does any error occurs?

Yes: Go to **Ext. FDD-7.**

No: The FDD assembly is faulty.
Change the FDD assembly with spare one.

FDD cable change

The FDD PCB and EXT. FDD cable are still suspected. In this entry, you will isolate the faulty component from them.

1. Turn OFF the power switches of the Ext. FDD and the T1100 PLUS System Unit.
2. Change the Ext. FDD cable with good one for checking.
3. Turn ON the power switches of the Ext. FDD and the T1100 PLUS System Unit then run the FDD test program for Ext. FDD.

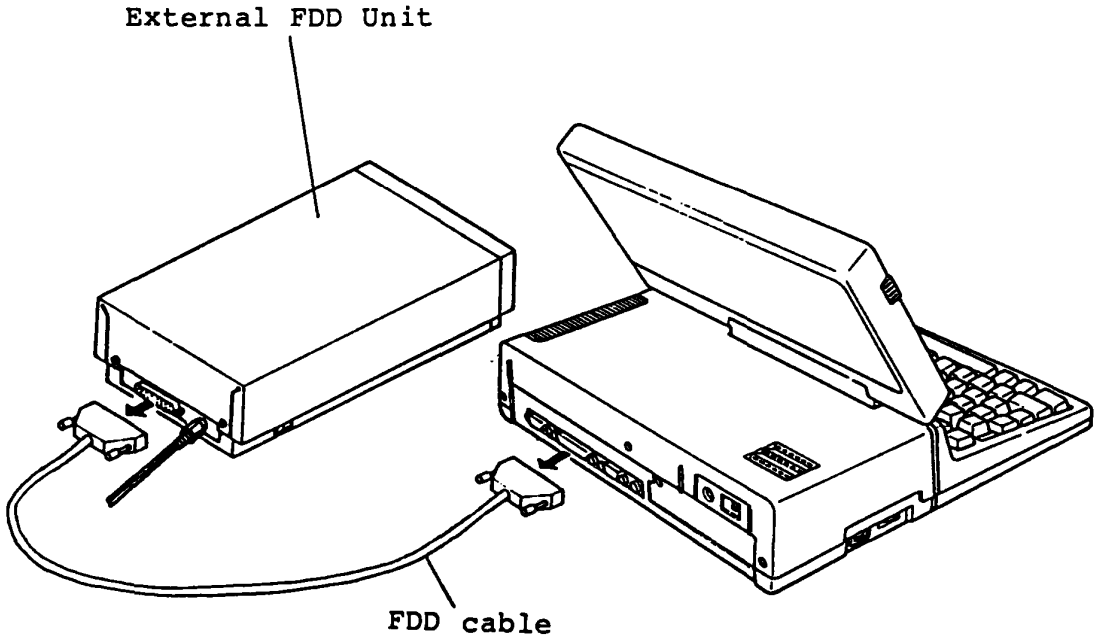


Figure 4-39 FDD Cable Change

Does any error occurs?

Yes: Go to **Ext. FDD-8.**

No: The Ext. FDD cable is faulty.
Change the Ext. FDD cable with spare one.

FDD PCB change

The FDD PCB is suspected.
Change the FDD PCB (FFD5C1) refering to PART 5: REPLACEMENT /ADJUSTMENT.

1. Turn OFF the power switches of the Ext. FDD and the T1100 PLUS System Unit.

2. Replace the Ext. FDD PCB then run FDD test program for the Ext. FDD.

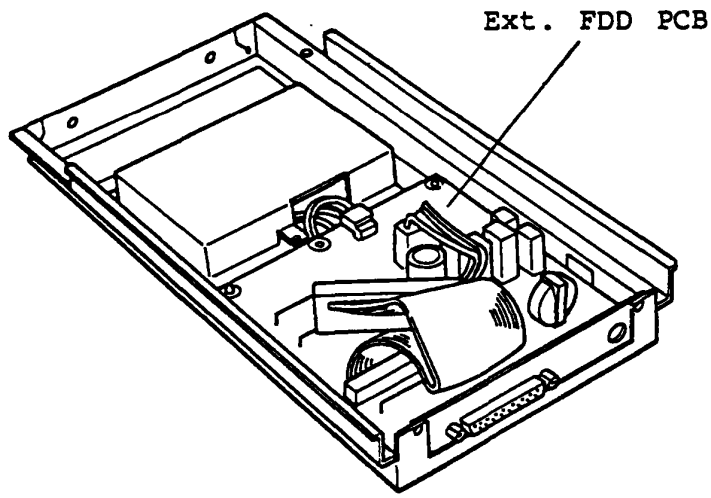


Figure 4-40 FDD PCB Change

Does any error occurs?

Yes: Ext. FDD UNIT is good.
The System board of the T1100 PLUS System Unit is suspected.
Go to the TIP of **System PCB.**

No: The FDD PCB of the Ext. FDD is faulty.
Change the FDD PCB.

5.1 DISASSEMBLING THE UPPER COVER OF THE SYSTEM UNIT

1. Turn OFF the power switch of the System Unit.
2. Turn the System Unit upside down, then remove the five screws (A) on the Lower Cover.
3. Turn the System Unit to normal position, then remove the three screws (B) on the rear panel of the System Unit.

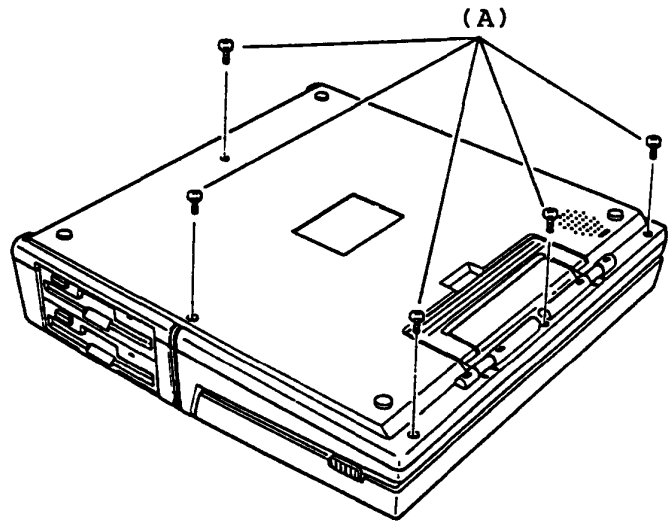


Figure 5-1 Five Scres Removal

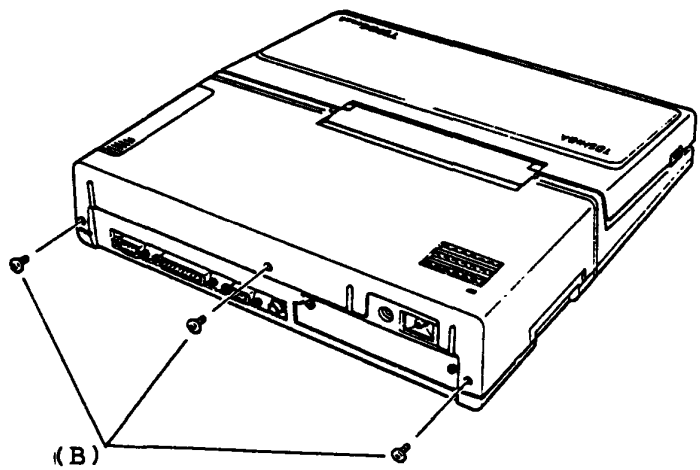


Figure 5-2 Three Screws removal

To be continued.

5.1 DISASSEMBLING THE UPPER COVER OF THE SYSTEM UNIT (Continued)

REMOVAL

4. Stand the Upper Cover (C) to left side of the System Unit as shown in the figure 5-3.

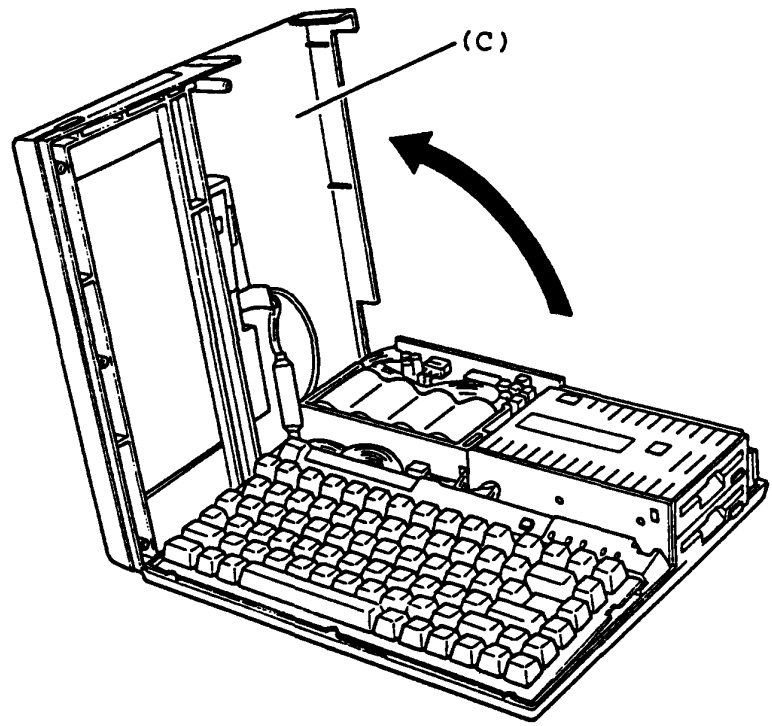


Figure 5-3 Disassemble the Upper Cover

REPLACEMENT

Follow the reverse procedure.

5.2 UPPER COVER REMOVAL/REPLACEMENT

REMOVAL

1. Turn OFF the power switch of the System Unit.
2. Disassemble the Upper Cover of the System Unit.
   (see section 5.1)
3. Lift up the Keyboard Unit, then put it in front of the System PCB (A).
4. Lift up the Indicator plate (B), then put it on the System PCB (A).
5. Disconnected the LCD cable (C) from the System PCB (A), then remove the one screw (D) from the System PCB (A) for disconnected the GND cable (E) of LCD Display to remove the Upper Cover (F).

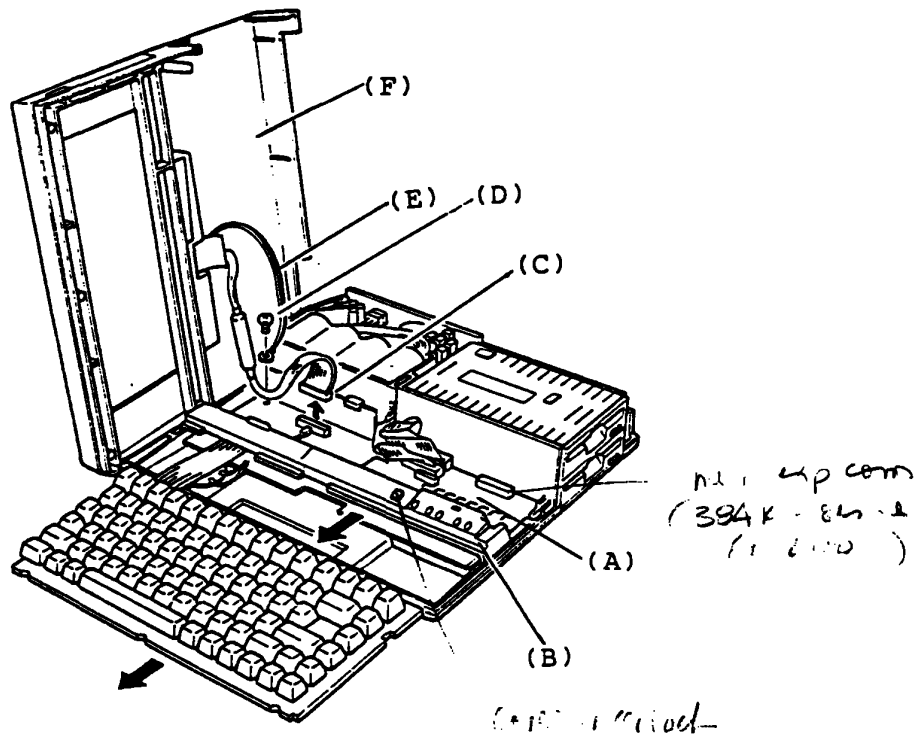


Figure 5-4 Upper Cover Removal

REPLACEMENT

Follow the reverse procedure.

5.3 KEYBOARD UNIT REMOVAL/REPLACEMENT

REMOVAL

1. Turn OFF the power switch of the System Unit.

2. Disassemble the Upper Cover of the System Unit.
(see section 5.1)

3. Lift up the Keyboard Unit (A), then put it in front of the System PCB (B).

4. Pull the pressure plate (C) of connector (PJ 1), then pull out the keyboard cable (D) from the System PCB (B) to remove the Keyboard Unit (A).

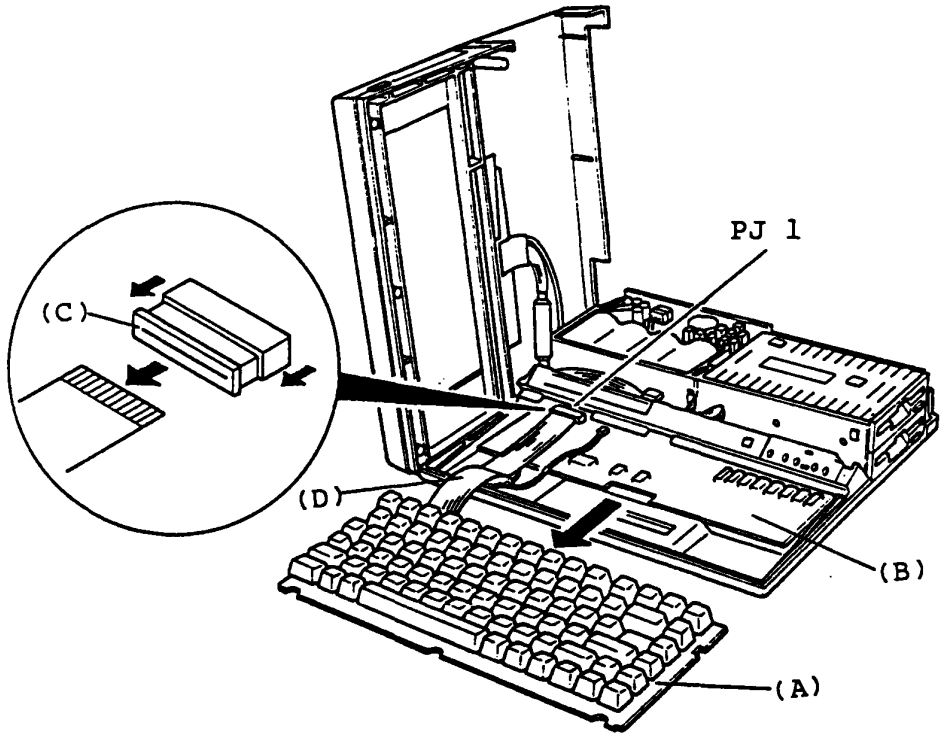


Figure 5-5 Keyboard Unit Removal

REPLACEMENT

Follow the reverse procedure.

The Keyboard cable (Flat cable) is fixed to the Keyboard connector with pressure plate. To connect the Keyboard connector insert the cable into the connector then press the pressure plate securely.

5.4 INDICATOR REMOVAL/REPLACEMENT

REMOVAL

1. Turn OFF the power switch of the System Unit.

2. Disassemble the Upper Cover of the System Unit. (see section 5.1)

3. Lift up the Keyboard Unit, then put it in front of the System PCB (A). (refer to figure 5-5)

4. Lift up the Indicator Plate (B), then disconnect the LED cable (C) from the System PCB (A) to remove it.

5. Remove the one screw (D) on the rear panel of the Indicator Plate (B) to remove the Indicator (E).

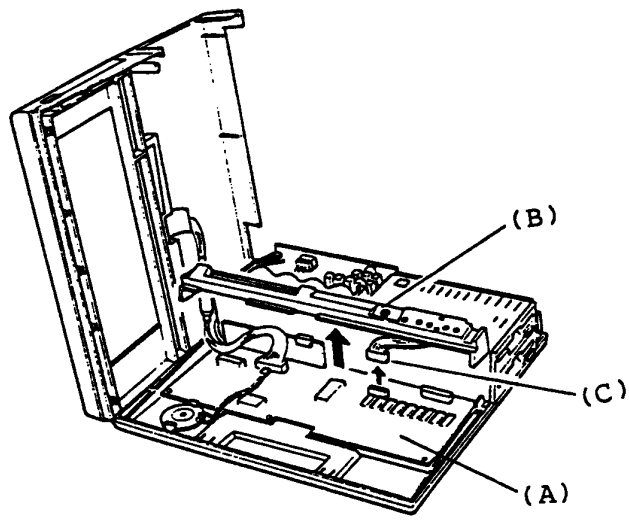


Figure 5-6 Indicator Plate Removal

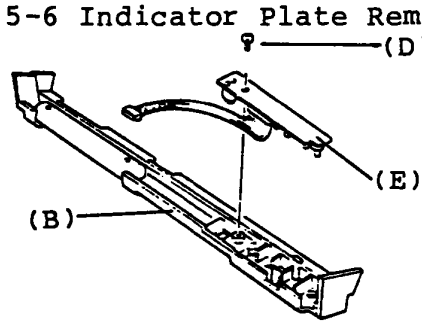


Figure 5-7 Indicator Removal

REPLACEMENT

Follow the reverse procedure.

5.5 BATTERY PACKAGE AND POWER SUPPLY PCB REMOVAL / REPLACEMENT

REMOVAL

1. Turn OFF the power switch of the System Unit.
2. Disassemble the Upper Cover of the System Unit.
   (see section 5.1)
3. Disconnect the three cables (A) from the Power Supply PCB (B).
4. Remove the Battery Package (C) on the FDD base (D).
5. Remove the two screws (E) on the rear panel of the System Unit to remove the filler panel (F).
6. Remove the three screws (G) on the Power Supply PCB (B), then remove the metal plate (I) to remove the Power Supply PCB.

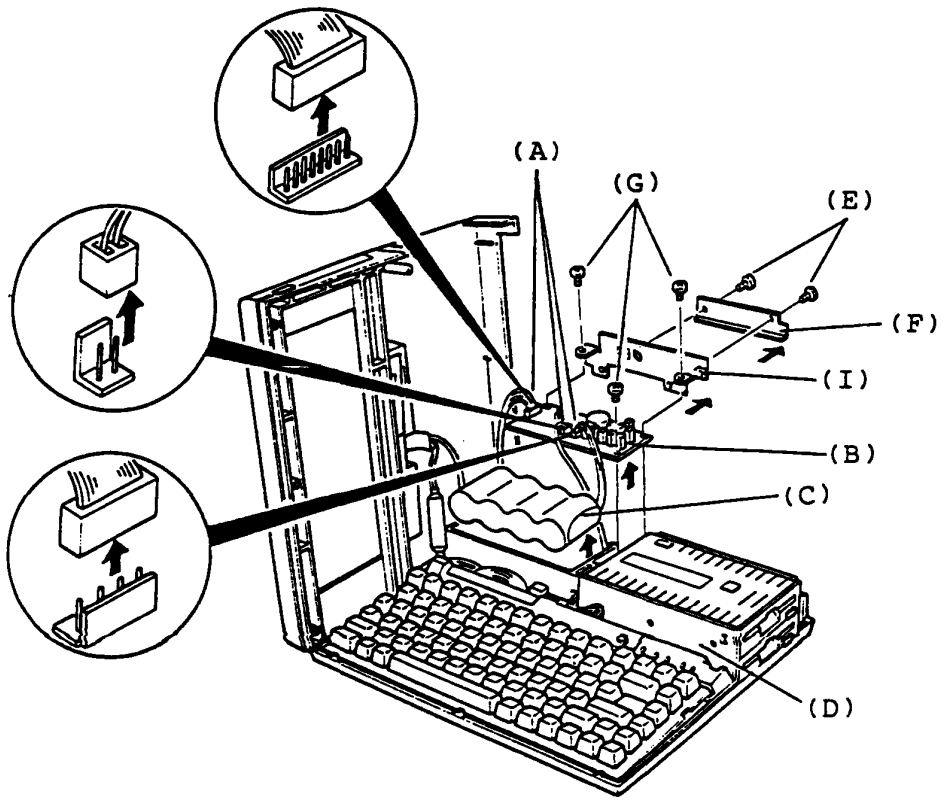


Figure 5-8 Battery Package and Power Supply PCB Removal

RPLACEMENT

Follow the reverse procedure.

5.6 FLOPPY DISK DRIVE BASE REMOVAL/REPLACEMENT

REMOVAL

1. Turn OFF the power switch of the System Unit.
2. Disassemble the Upper Cover of the System Unit. (see section 5.1)
3. Remove the Keyboard Unit and Indicater Plate from the System PCB. (see section 5.3, 5.4)
4. Disconnected the FDD cable(s) (A) from the System PCB (B).
5. Remove the four screws (C)(D) on the FDD base (E) to remove the FDD baes (E).

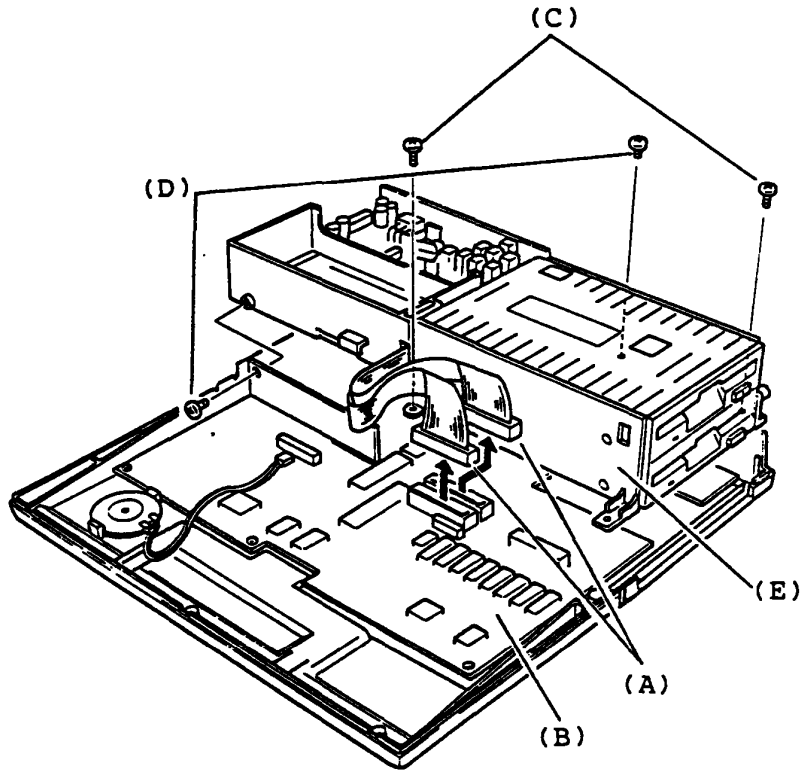


Figure 5-9 FDD Base Removal

REPLACEMENT

Follow the reverse procedure.
Screws (D) is short screw.

5.7 FLOPPY DISK DRIVE REMOVAL/REPLACEMENT

REMOVAL

1. Turn OFF the power switch of the System Unit.

2. Disassemble the Upper Cover of the System Unit.
(see section 5.1)

3. Remove the Keyboard Unit, Indicator plate and FDD base from the System Unit. (see section 5.3, 5.4, 5.6)

In the case of the F type

4. Remove the four screws (A)(B) on the FDD base (C), then remove the metal plate (D) and Floppy Disk Drive (E).

5. Push the both side nales of the filler panel (F), then remove it.

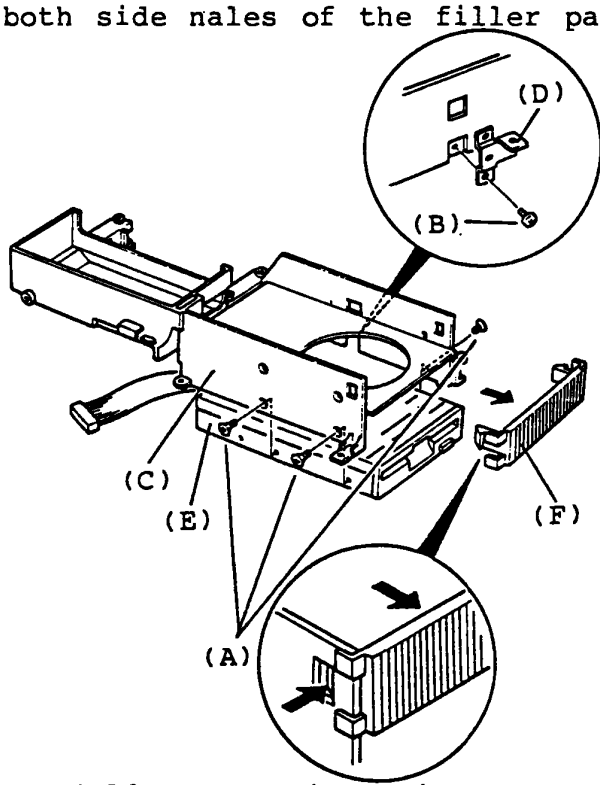


Figure 5-10 Floppy Disk Drive Removal (F type)

REPLACEMENT

Follow the reverse procedure.
Screws (A) is flat head screws.

To be continued.

5.7 FLOPPY DISK DRIVE REMOVAL/REPLACEMENT (Continued)

REMOVAL

In the case of the F/F type

4. Remove the eight screws (G)(H) on the FDD base, then remove the metal plate (I) and bottom Floppy Disk Drive (J).

5. Pass the FDD cable through a slit of the FDD base to remove the top Floppy Disk Drive (K).

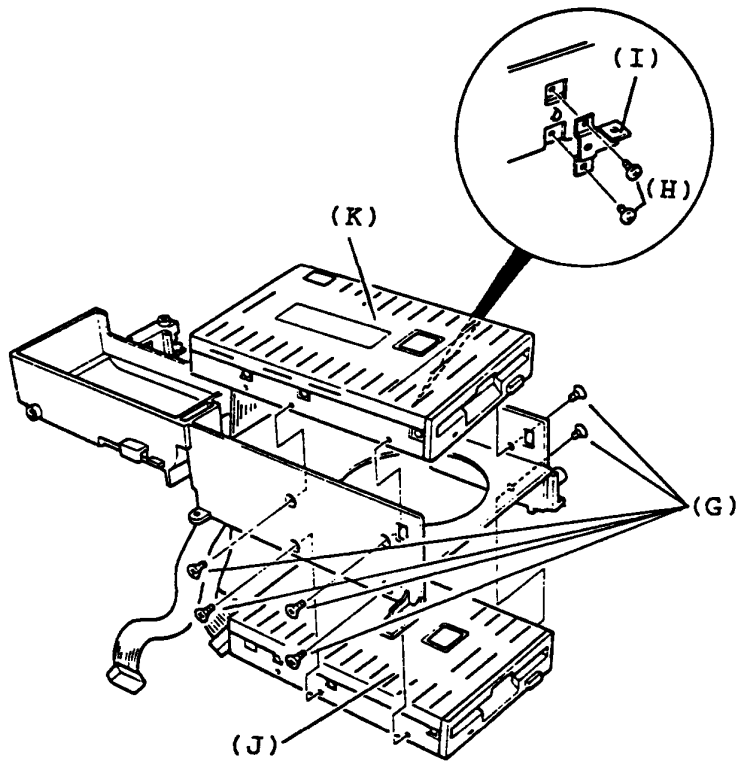


Figure 5-11 Floppy Disk Drive Removal (F/F type)

REPLACEMENT

Follow the reverse procedure.
Screws (G) is flat head screw.

5.8 FDD BEZEL REMOVAL/REPLACEMENT

REMOVAL

1. Turn OFF the power switch of the System Unit.

2. Remove the Upper Cover, Keyboard Unit, Indicator plate, FDD base and FDD. (see section 5.2, 5.3, 5.4 5.6, 5.7)

3. Spread the four nailes (A) with the blade scrwdriver to remove the FDD cover as shown in the figure 5-12.

4. Remove the two screws (B) on the FDD device (C) to remove the FDD bezel (D).

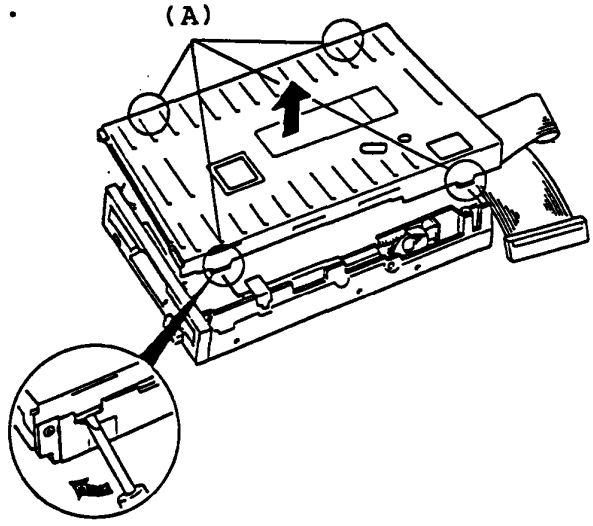


Figure 5-12 Spreading the Nailes

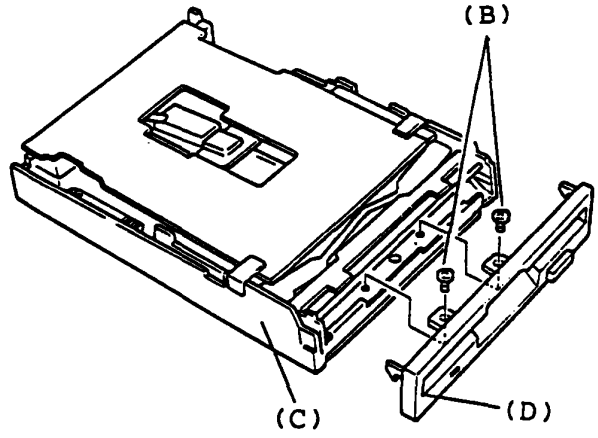


Figure 5-13 FDD Bezel Removal

REPLACEMENT

Follow the reverse procedure.

5.9 SYSTEM PCB REMOVAL/REPLACEMENT

REMOVAL

1. Turn OFF the power switch of the System Unit.
2. Remove the Upper Cover, Keyboard Unit, indicator plate and FDD base (see section 5.2, 5.3, 5.4, 5.6)
3. Remove the Expansion slot PCB (A) from the System PCB (B).
4. Disconnected the Speaker cable (C) from the System PCB (B).
5. Remove the three screws (D) on the System PCB (B) to remove the System PCB (B).

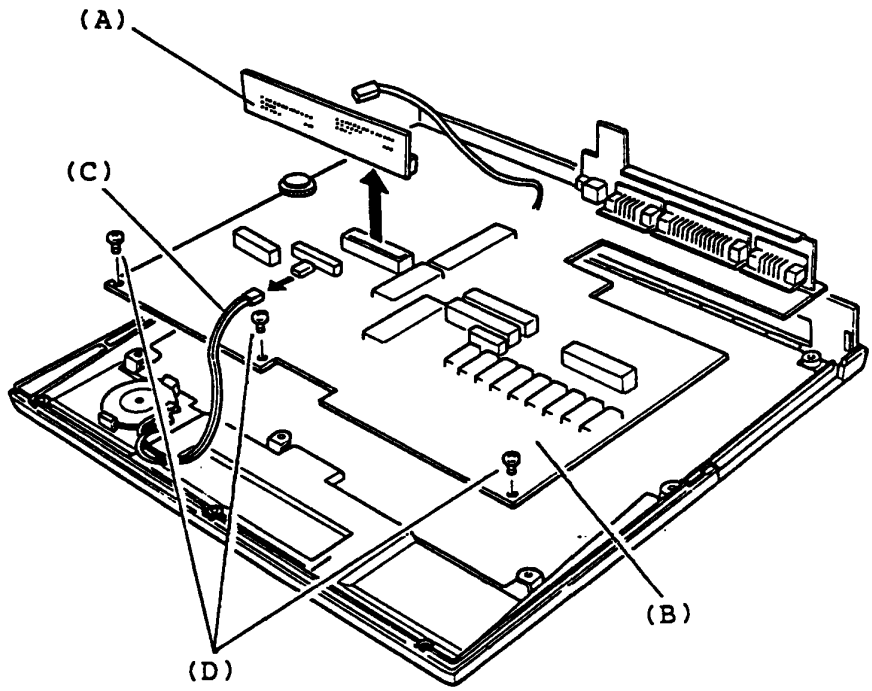


Figure 5-14 System PCB Rempval

REPLACEMENT

Follow the reverse procedure.

5.10 SPEAKER AND INSULATER REMOVAL/REPLACEMENT

REMOVAL

1. Turn OFF the power switch of the System Unit.

2. Remove the Upper Cover, Keyboard Unit, Indicator plate, FDD base and System PCB. (see section 5.2, 5.3, 5.4, 5.6, 5.9)

3. The speaker (A) is mounted on the Lower Cover (B) with a locking lever (C). Push the locking lever (C) outward so that the speaker is free to move, then pull out the speaker (A) from the Lower Cover (B).

4. Peel the Insulater (D) to remove it.

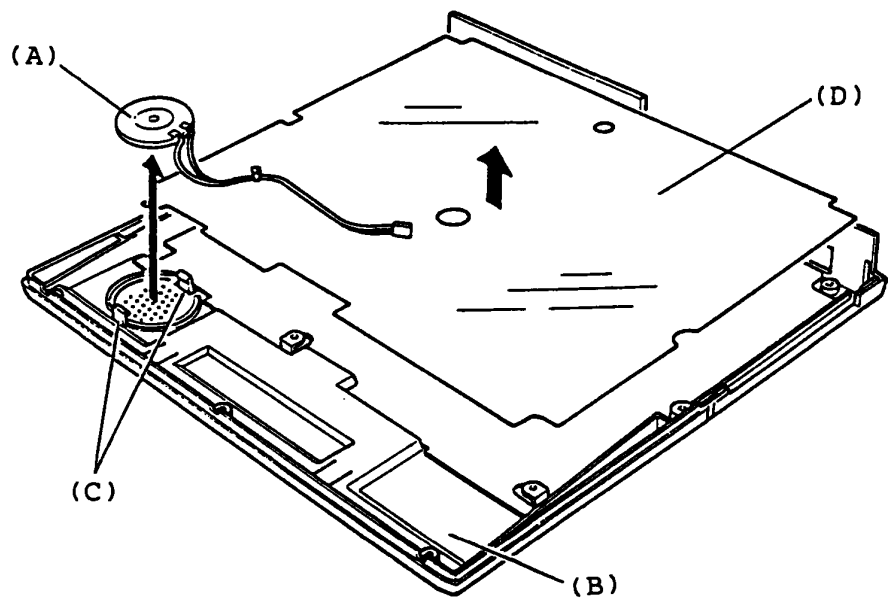


Figure 5-15 Speaker and Insulater Removal

REPLACEMENT

Follow the reverse procedure.

5.11 LCD MASK REMOVAL/REPLACEMENT

REMOVAL

1. Turn OFF the power switch of the System Unit.

2. Replace the latches (A) by sliding them forward hold the latches and pull up the display, then open the LCD as shown in the figure 5-16.

3. Peel the seal (B) from LCD Mask (C) with a pear of tweezers and remove it.

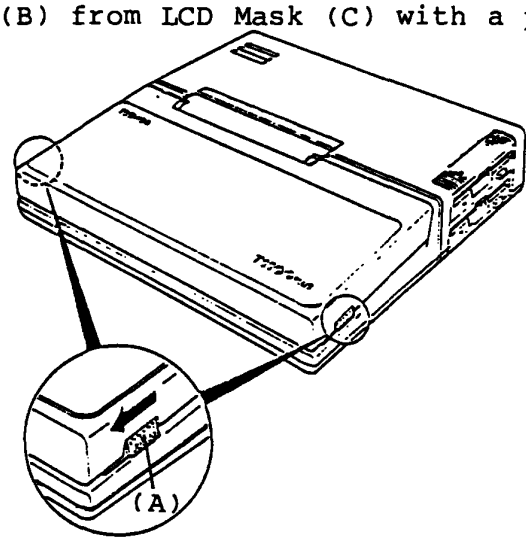


Figure 5-16 Opening the LCD

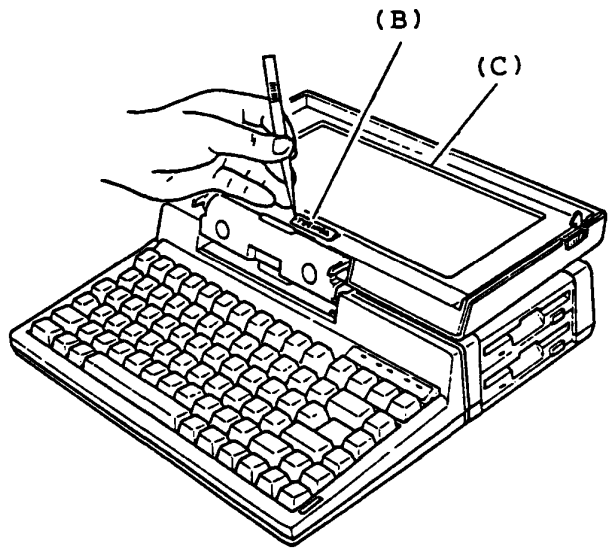


Figure 5-17 Peeling the Seal

To be continued.

5.11 LCD MASK REMOVAL/REPLACEMENT (Continued)

REMOVAL

4. Remove the one screw (D) from the LCD Mask (E), then slide the LCD Mask (E) to the forward position a little to remove it.

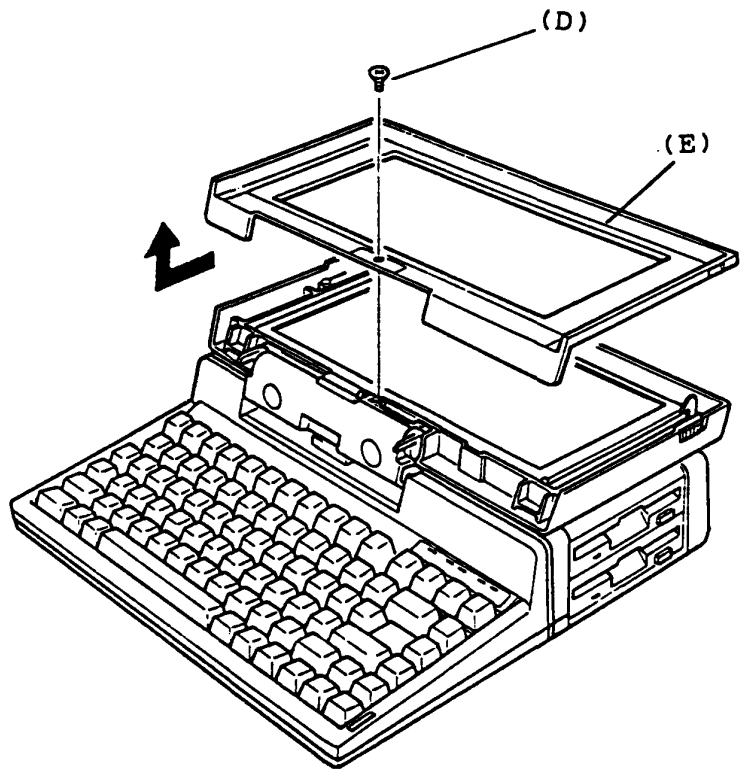


Figure 5-18 LCD Mask Removal

REPLACEMENT

Follow the reverse procedure.

5.12 LCD REMOVAL/REPLACEMENT

REMOVAL

1. Turn OFF the power switch of the System Unit.
2. Remove the LCD Mask from the System Unit.
(see section 5.11)
3. Remove the four screws (A) on the LCD (B).
4. Lift up the LCD (B), then put it on the Keyboard Unit.
5. Disconnect the LCD cable (C) from the rear of the LCD to remove the LCD (B).

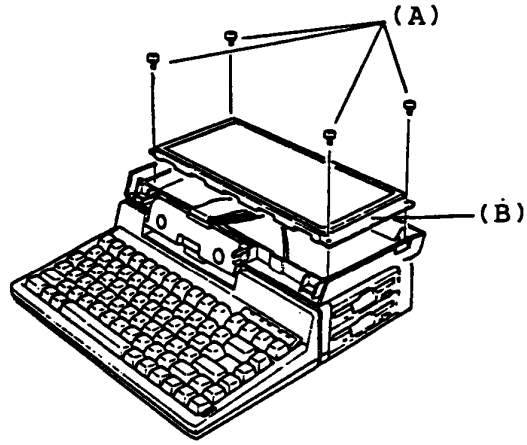


Figure 5-19 Four Screws Removal

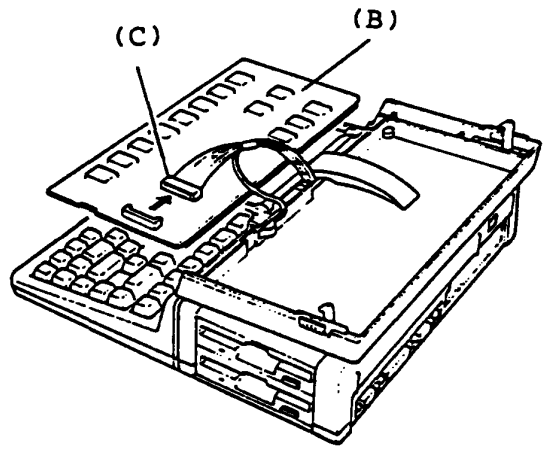


Figure 5-20 LCD Removal

REPLACEMENT

Follow the reverse procedure.

5.13 LCD REAR COVER REMOVAL/REPLACEMENT

REMOVAL

1. Turn OFF the power switch of the System Unit.
2. Remove the LCD Mask and LCD. (see section 5.11, 5.12)
3. Peel the seal (A) with a pair of tweezers from the hinge (B), then remove it.
4. Peel the LCD GND cable (C) from the LCD rear cover (D).
5. Remove the two screws (E) on the hinge (B).

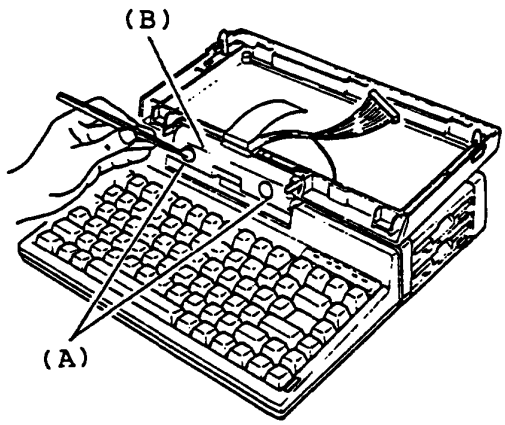


Figure 5-21 Peeling the Seal

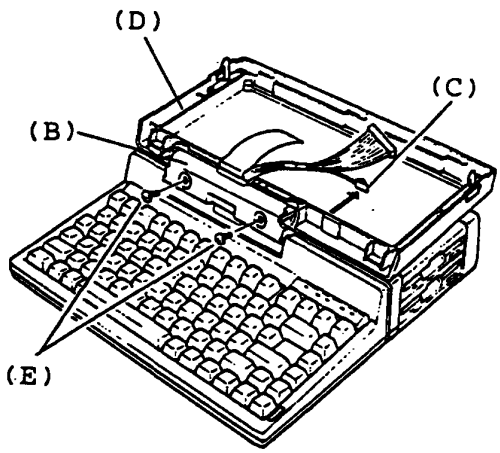


Figure 5-22 Two Mounting Screws Removal

To be continued.

5.13 LCD REAR COVER REMOVAL/REPLACEMENT (Continued)

REMOVAL

5. Turn the LCD rear cover down, then remove the hinge (E) from the Upper Cover (F).

6. Pull out the torsion bar (G) from hole of the Upper Cover (H).

7. Remove the LCD rear cover (I) to forward position.

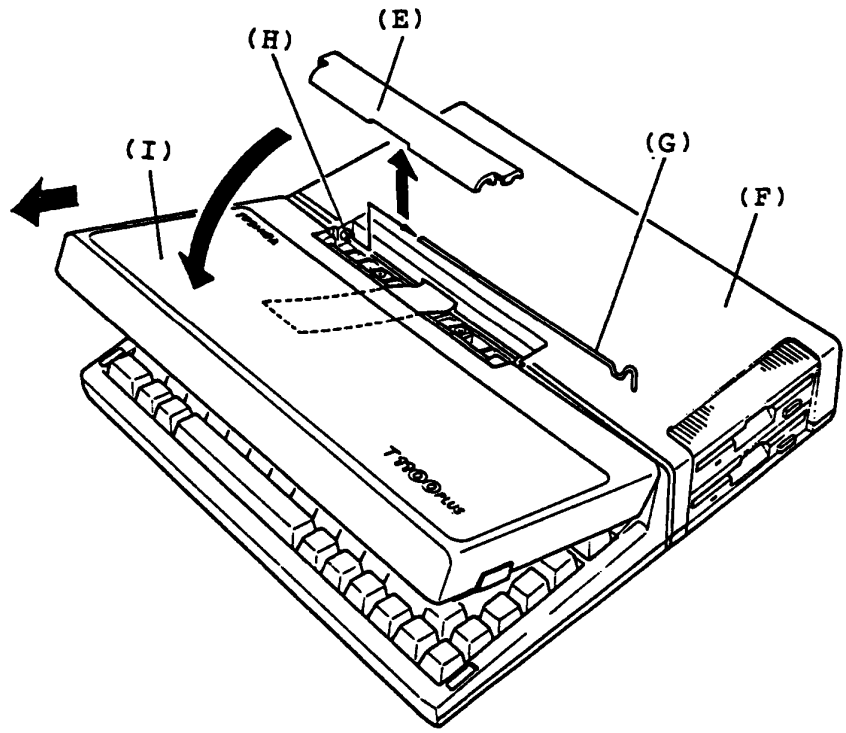


Figure 5-23 LCD Rear Cover Removal

REPLACEMENT

Follow the reverse procedure.

5.14 MEMORY CARD REMOVAL/REPLACEMENT (Option)

REMOVAL

1. Turn OFF the power switch of the System Unit.
2. Disassemble the Upper Cover of the System Unit.
(see section 5.1)
3. Lift up the Keyboard Unit and Indicator plate, put it front of the System PCB (A) as shown in the figure 5-24.
4. Pull out the Memory Card (B) from the System PCB (A).
5. If the memory size of the T1100 PLUS System have been changed you must change the setting of configuration DIP switch (C).
(Refer to page 1-10)

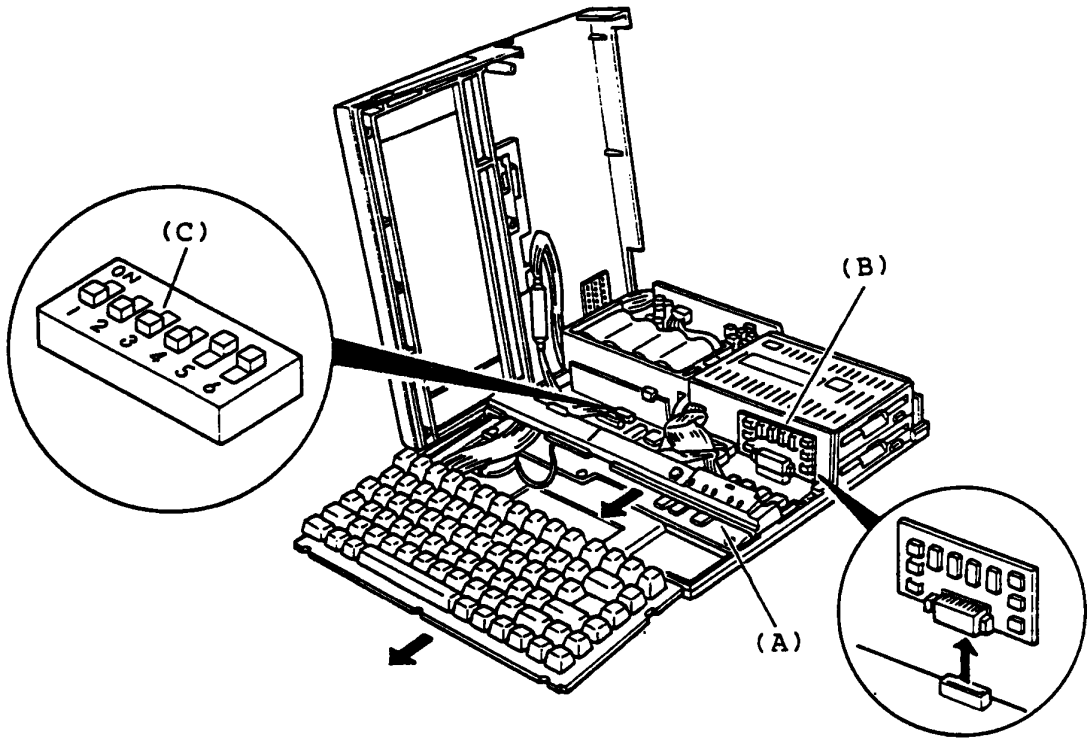


Figure 5-24 Memory Card Removal

REPLACEMENT

Follow the reverse procedure.

5.15 MODEM CARD AND I/O EXPANSION CARD REMOVAL/REPLACEMENT (Option)

REMOVAL

1. Turn OFF the power switch of the System Unit.
2. Remove the two screws (A) fixing the Modem Card (B).
3. Hook the card puller (C) into the holes (D).
4. Hold the card puller (C) and gently slide out the card.

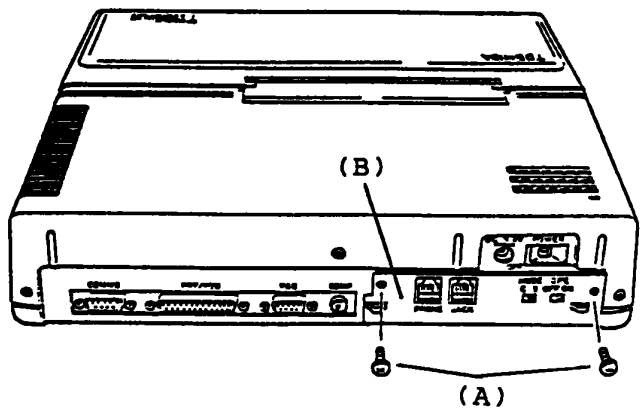


Figure 5-25 Two Screws Removal

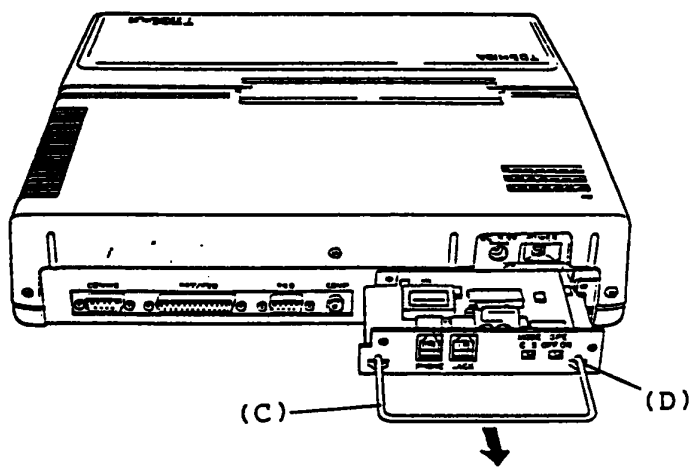


Figure 5-26 Modem Card or I/O Expansion Card Removal

REPLACEMENT

Follow the reverse procedure.

5.16 5.25" EXTERNAL FDD DISASSEMBLE/ASSEMBLE (option)

Upper Cover Removal/Replacement

REMOVAL

1. Turn OFF the power switch of the Ext. FDD (External FDD) and the System Unit then remove the Ext. FDD cable from the rear of the Ext. FDD Unit.

2. Remove four screws (A) from the Ext. FDD.

3. Slide the Upper Cover (B) backward to remove it.

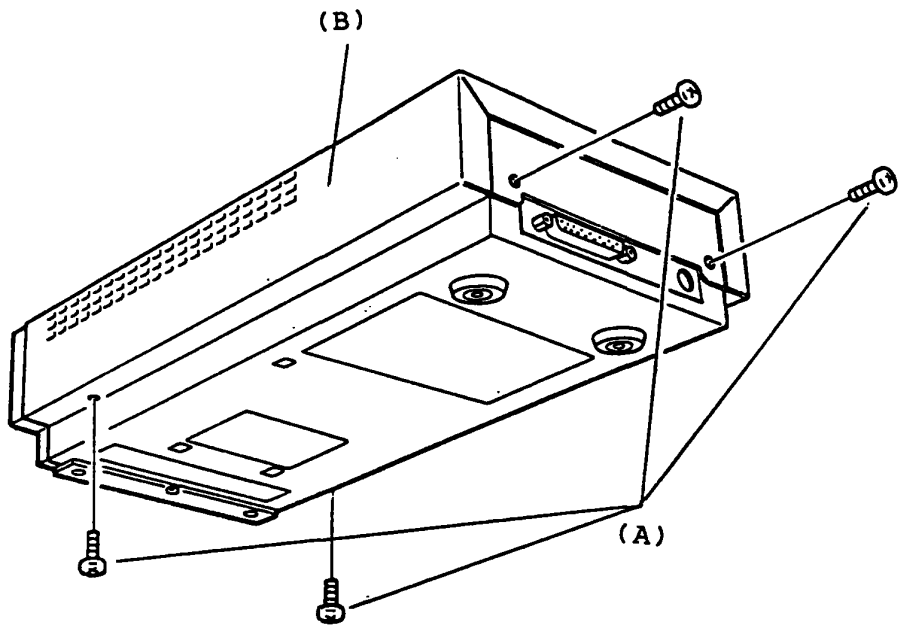


Figure 5-27 Upper Cover Removal

REPLACEMENT

Follow the reverse procedure.

5.16 5.25" EXTERNAL FDD DISASSEMBLE/ASSEMBLE (Continued)

FDD Assembly (and Front Panel) Removal/Replacement

REMOVAL

1. Remove three screws (A) of the FDD assembly.
2. Disconnect the signal cable connector J2 (B) and power cable connector J1 (C) on the FDD assembly.
3. Slide the FDD assembly forward to remove it.
4. The FDD assembly has a front panel (D) which is mounted to the FDD assembly by two screws (E).
   Remove the two screws (E) to remove the front panel if need.

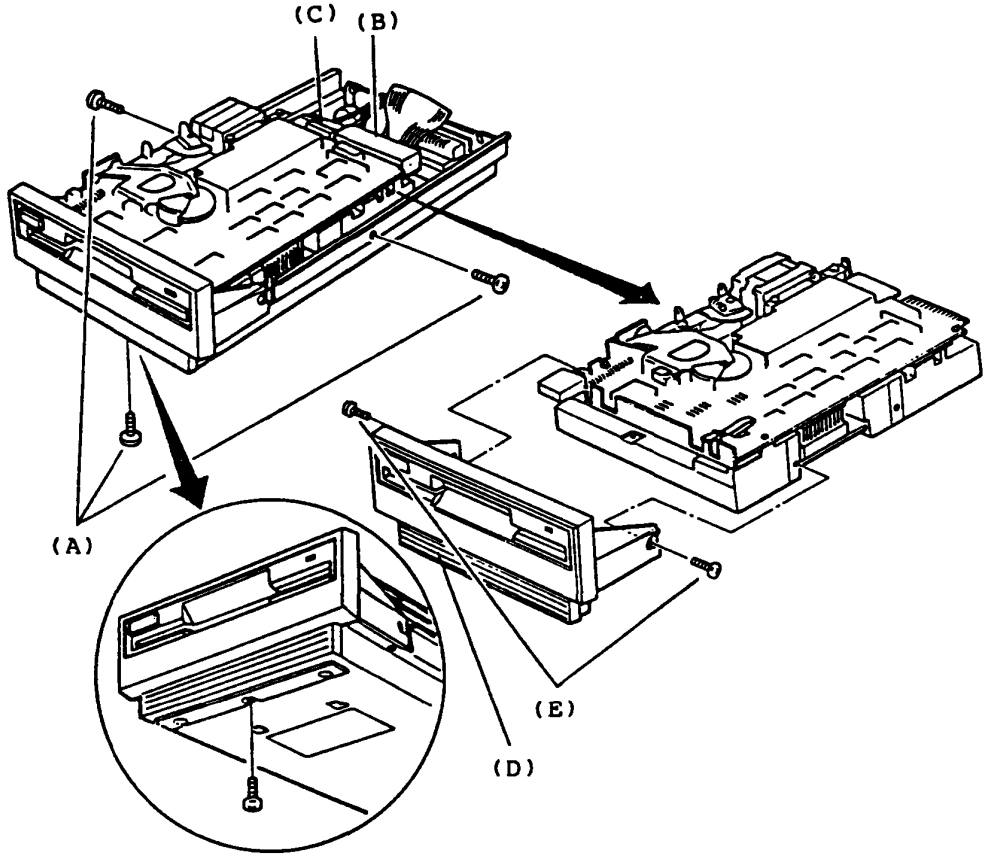


Figure 5-28 FDD Assembly Removal

REPLACEMENT

Follow the reverse procedure.

5.16 5.25" EXTERNAL FDD DISASSEMBLE/ASSEMBLE (Continued)

FDD PCB (FFD5C1) Removal/Replacement

REMOVAL

1. Disconnect the battery connector PJ4 (A) on the FDD PCB.

2. The FDD PCB (B) is mounted on the lower cover with a nylon latch (C) and a slot (D).
   Nip head of the nylon latch on the PCB by a longnose plier to be free then lift the PCB up by getting it out of the slit.

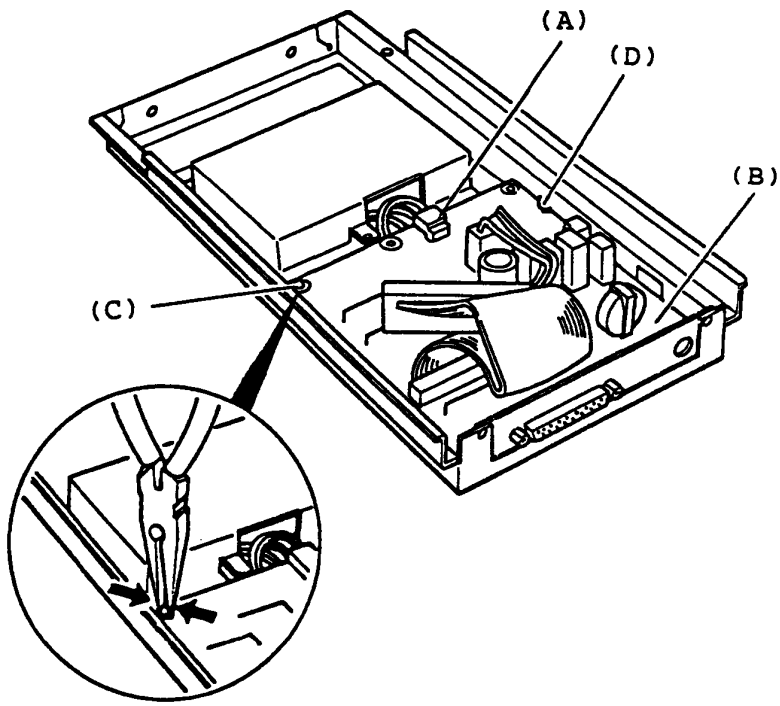


Figure 5-29 FDD PCB Removal

REPLACEMENT

Follow the reverse procedure.

5.16 5.25" EXTERNAL FDD DISASSEMBLE/ASSEMBLE (Continued)
Battery Removal/Replacement

REMOVAL

The battery stock room is there under the FDD assembly..
Before removing the battery, you have to remove the FDD assembly and disconnect the battery connector PJ4 on the FDD PCB.

1. Remove the battery cover screw (A).

2. Slide the battery cover (B) backward one inch to unhoock then lift up the battery cover. You can access the battery.

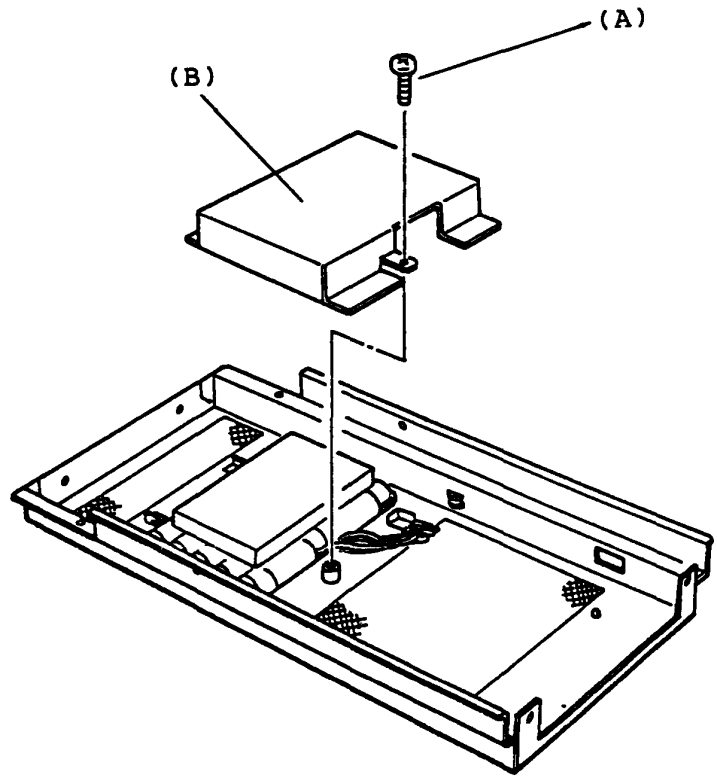


Figure 5-30 Battery Removal

REPLACEMENT

Follow the reverse procedure.

PART 6 LOCATION

CONTENTS

SYSTEM UNIT (Front View)

(A) System PCB

(B) Memory Card (Option)

(C) 3.5" Floppy Disk Drive
F type ..... One Floppy Disk Drive
F/F type ... Two Floppy Disk Drive

(D) Keyboard

(E) Power Supply Unit

(F) Speaker

(G) LCD Display

(H) Upper Cover

(I) Lower Cover

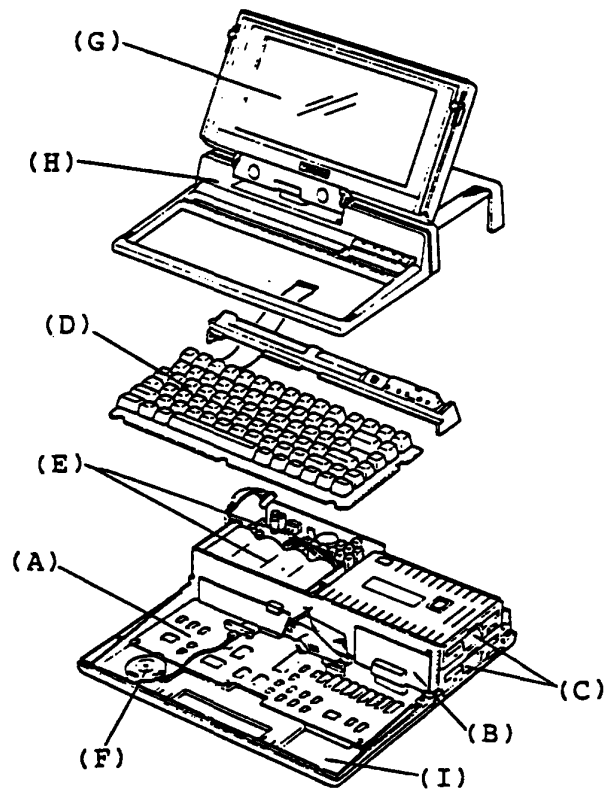


Figure 6-1 Front View of System Unit

SYSTEM UNIT (Rear Panel)

(A) Power Switch

(B) DC Jack

(C) Display Connector (for Color Display)

(D) Display Connector (for Monochrome Display)

(E) Printer or Expansion FDD Connector

(F) RS232C Cable Connector

(G) Modem Card or Interface Card Slot

(H) Printer / FDD Select Switch

(I) LCD Contrast Volume

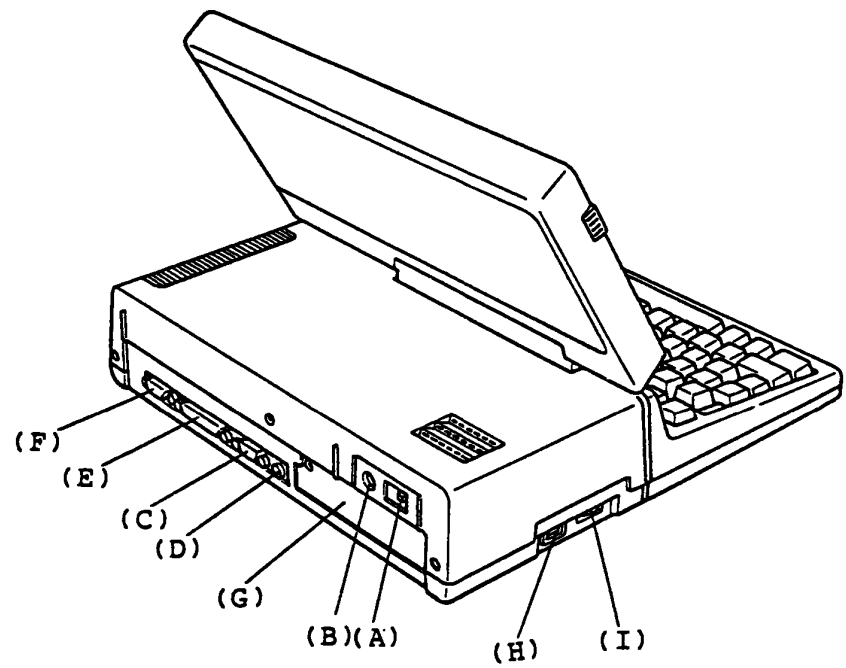


Figure 6-2 Rear Panel of System Unit

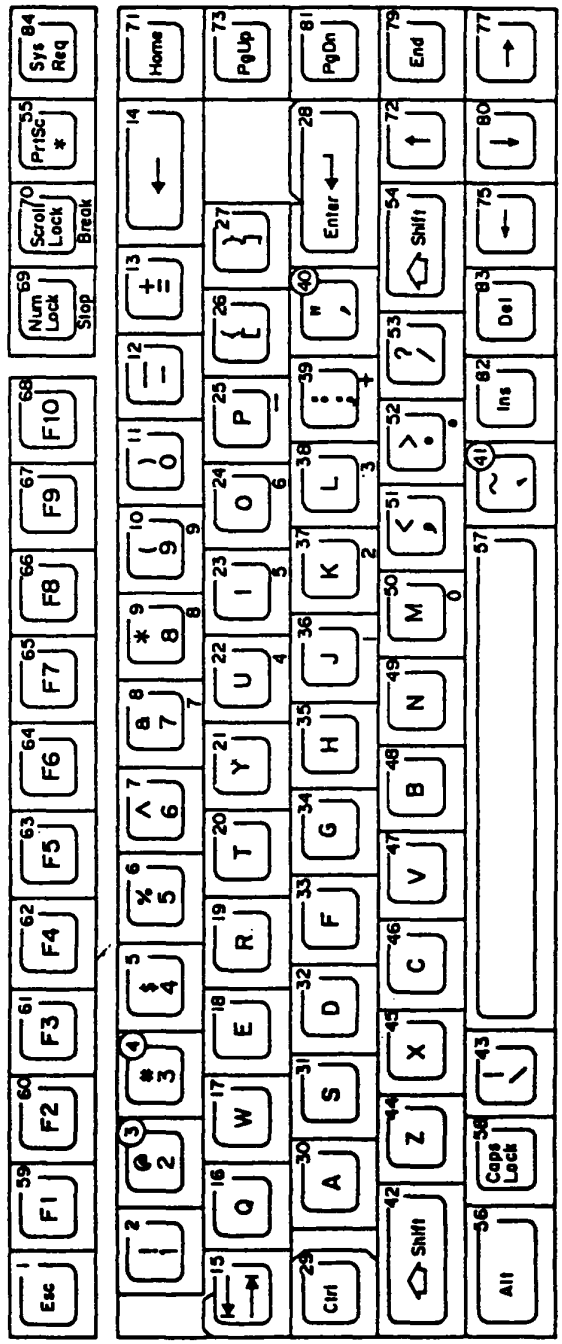


Figure 6-3 U.S.A. Version

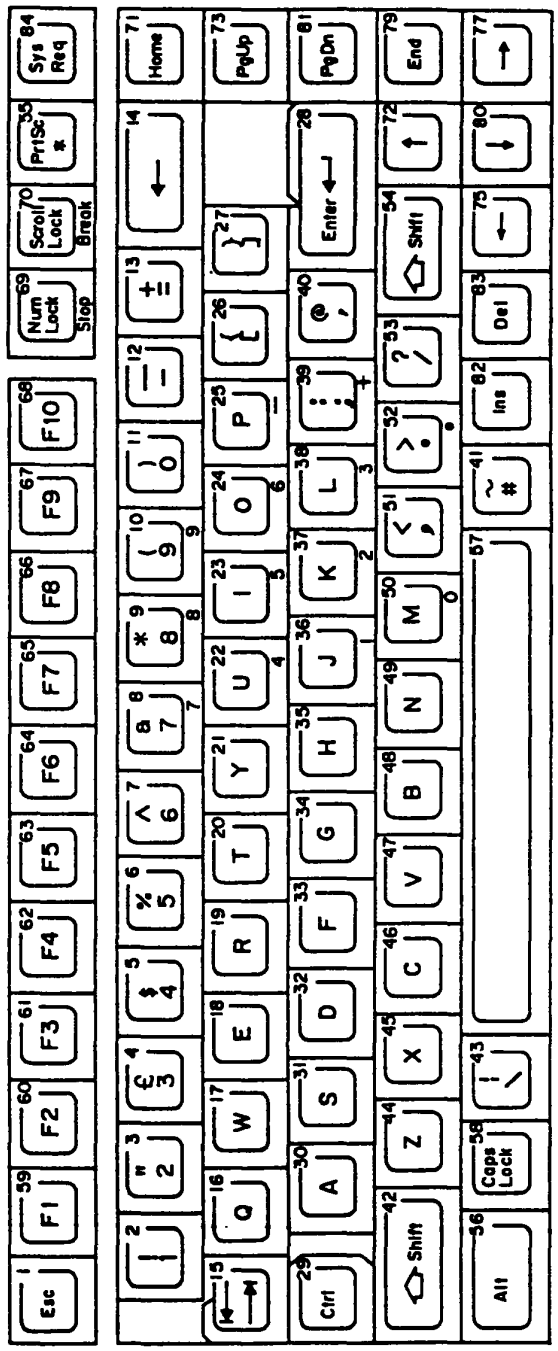


Figure 6-4 U.K. Version

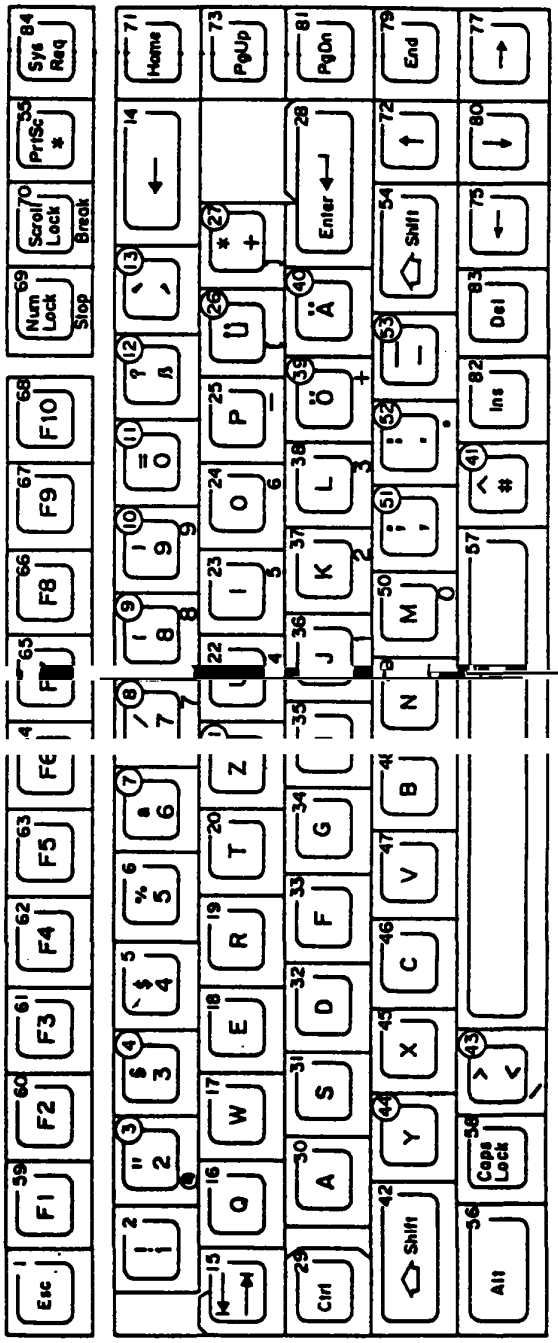


Figure 6-5 German Version

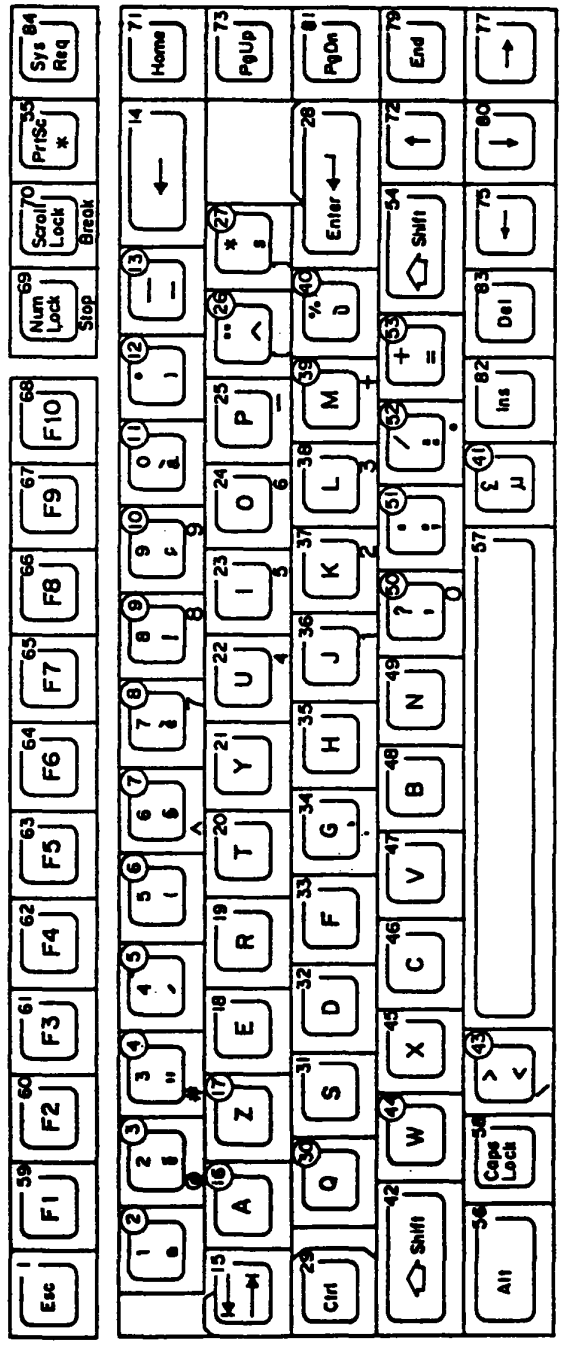


Figure 6-6 French Version

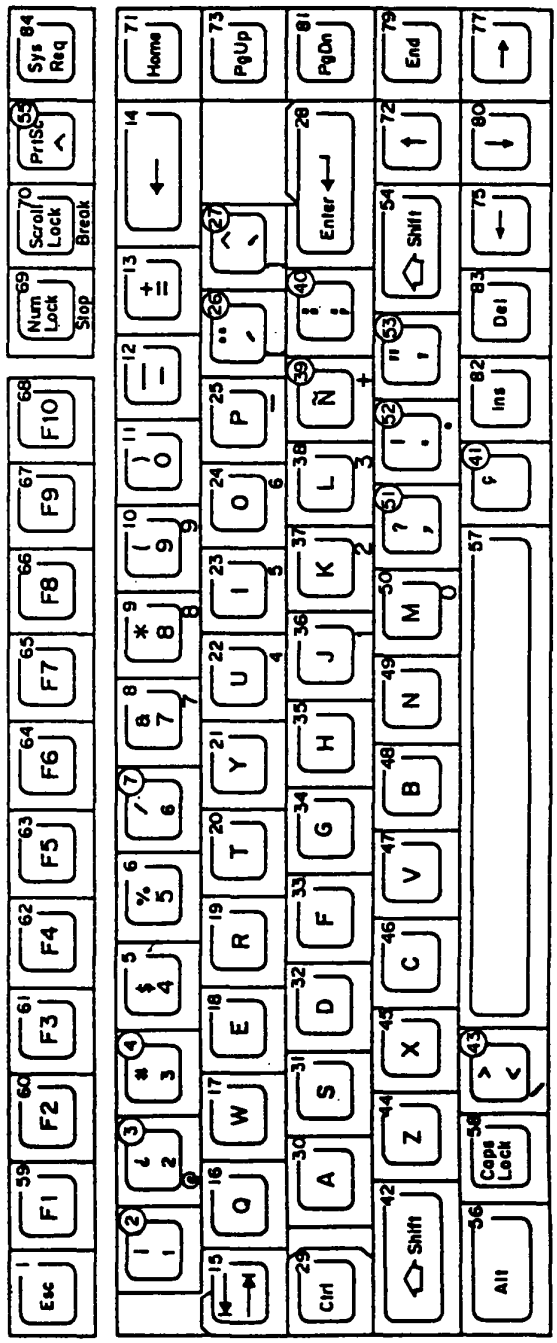


Figure 6-7 Spanish Version

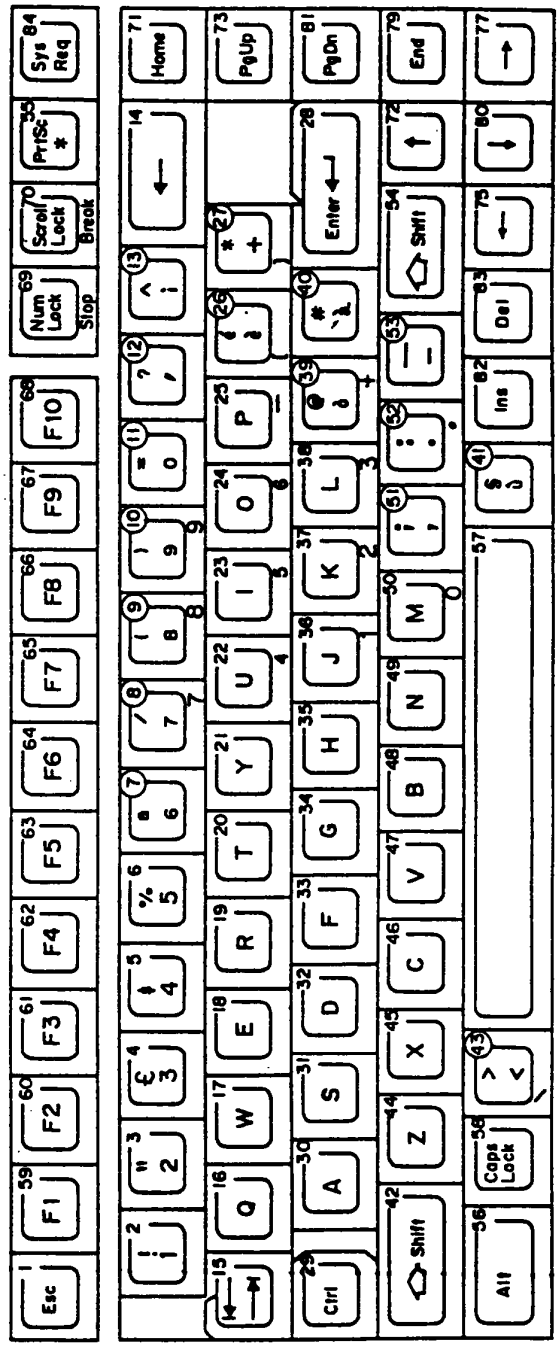


Figure 6-8 Italian Version

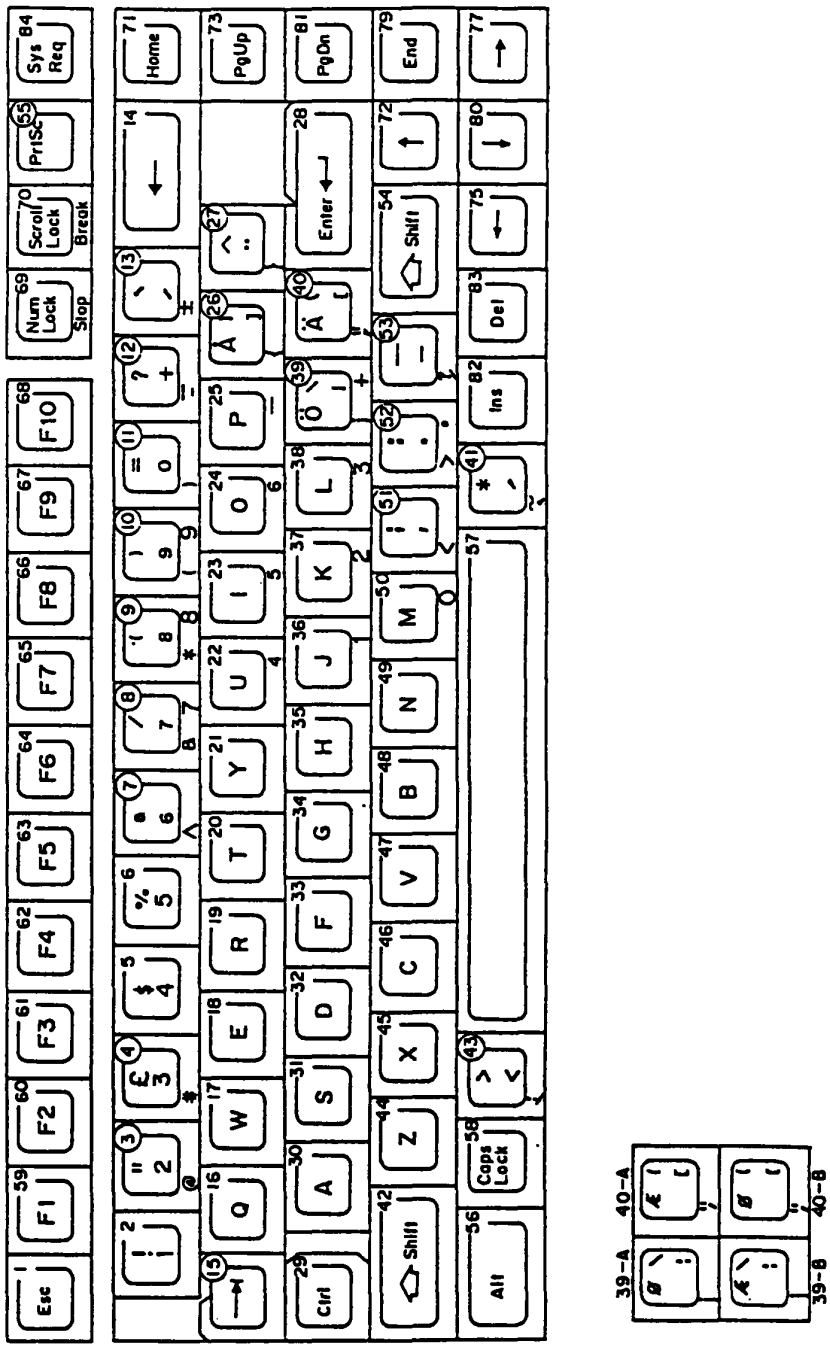
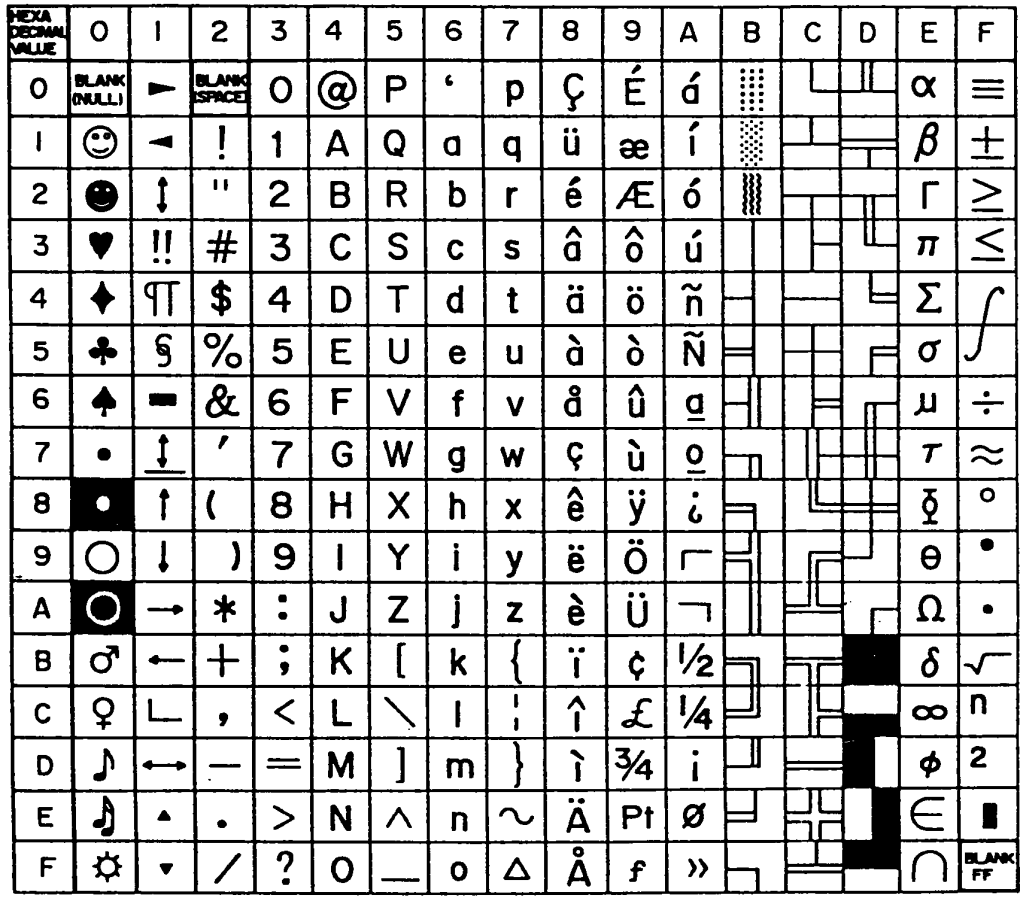


Figure 6-9 Scandinavian Version

Table 6-1 Code Table



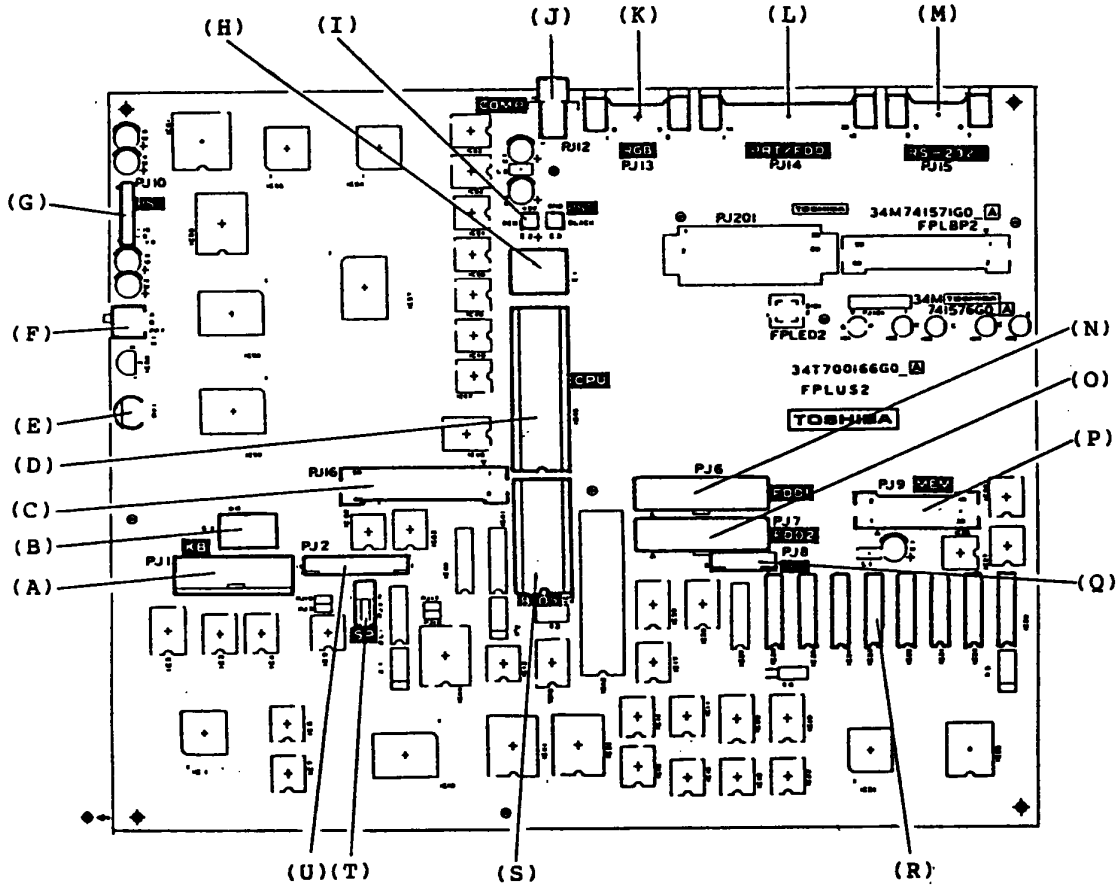


Figure 6-10 System PCB

(A) Keyboard Connector

(B) Configuration DIP Switch

(C) Expansion Bus Connector

(D) CPU

(E) LCD Contrast Volume

(F) Printer/FDD Select Switch

(G) Power Supply Connector 2

(H) Ni-Cd Battery

(I) Power Supply Connector 1

(J) Composit Video Connector

(K) Color CRT Display Connector

(L) External FDD and Printer Connector

(M) RS232C Connector

(N) FDD 1 Connector

(O) FDD 2 Connector

(P) Expansion Memory Connector

(Q) Indicator Connector

(R) Memory Chips (256 KB)

(S) ROM (BIOS)

(T) Speaker Connector

(U) LCD Connector

FLOPPY DISK DRIVE (FDD) (Top View of mechanical assembly)

(A) Head Assembly

(B) Stepping Motor

(C) Track 00 sensor

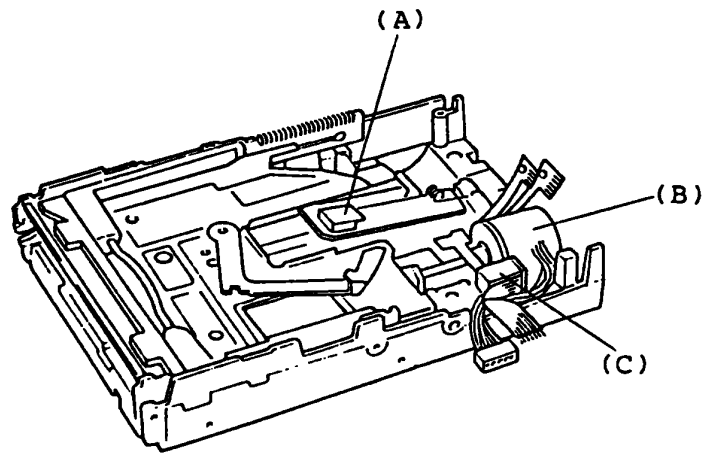


Figure 6-11 Top View of Mechanical Assembly

FLOPPY DISK DRIVE (FDD) (Bottom View)

(A) Drive Motor

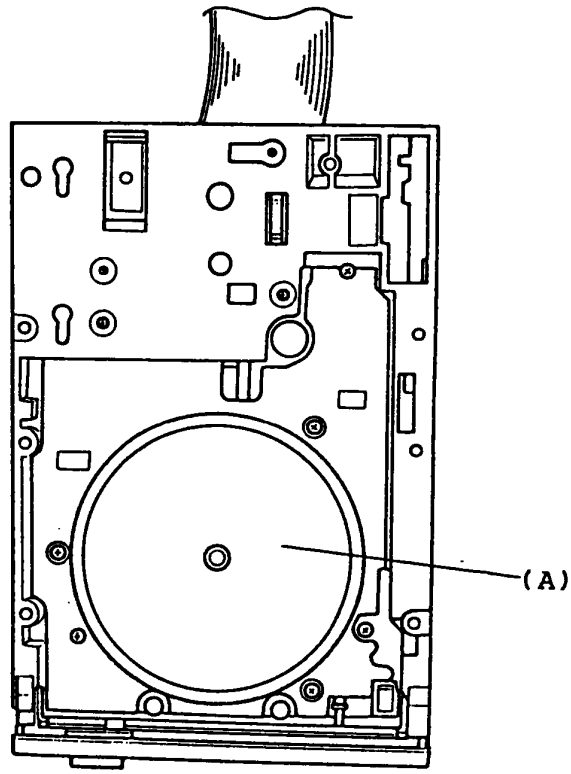


Figure 6-12 Bottom View of FDD

(A) PJ 2 Interface and power connector

(B) PJ 3 Sensor connector

(C) PJ 4 Sensor connector

(D) PJ 5 Step motor connector

(E) PJ 6 Read/Write head 0 connector

(F) PJ 7 Read/Write head 1 connector

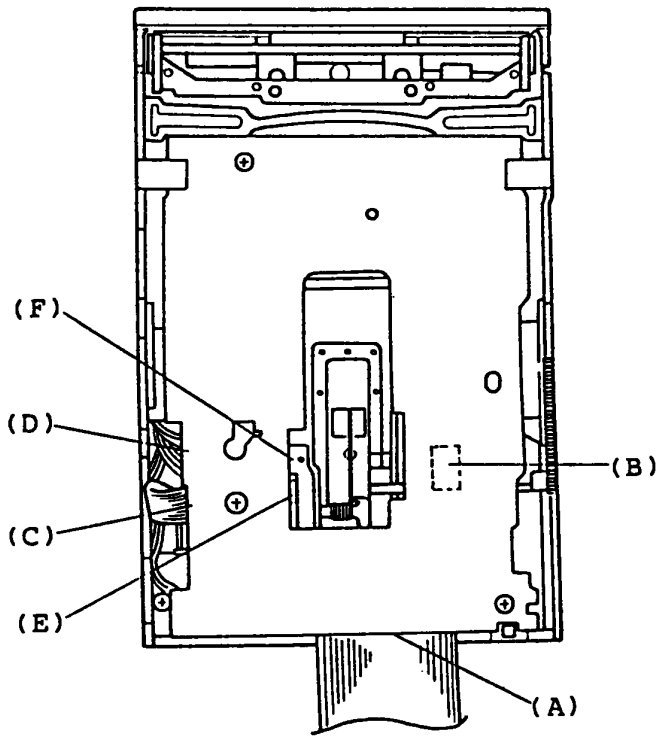


Figure 6-13 FDD PCB

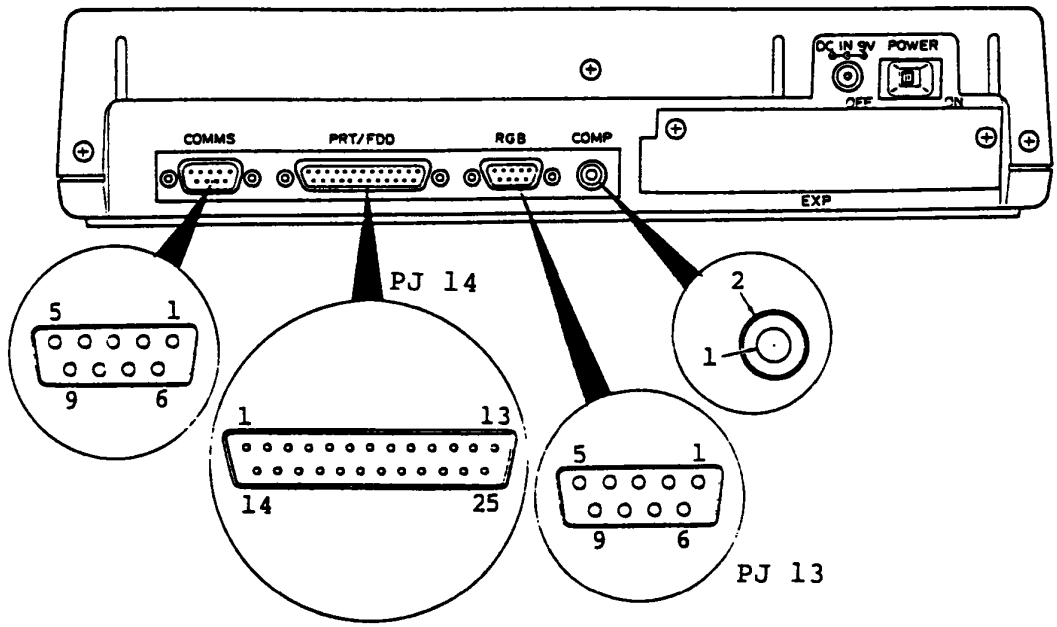


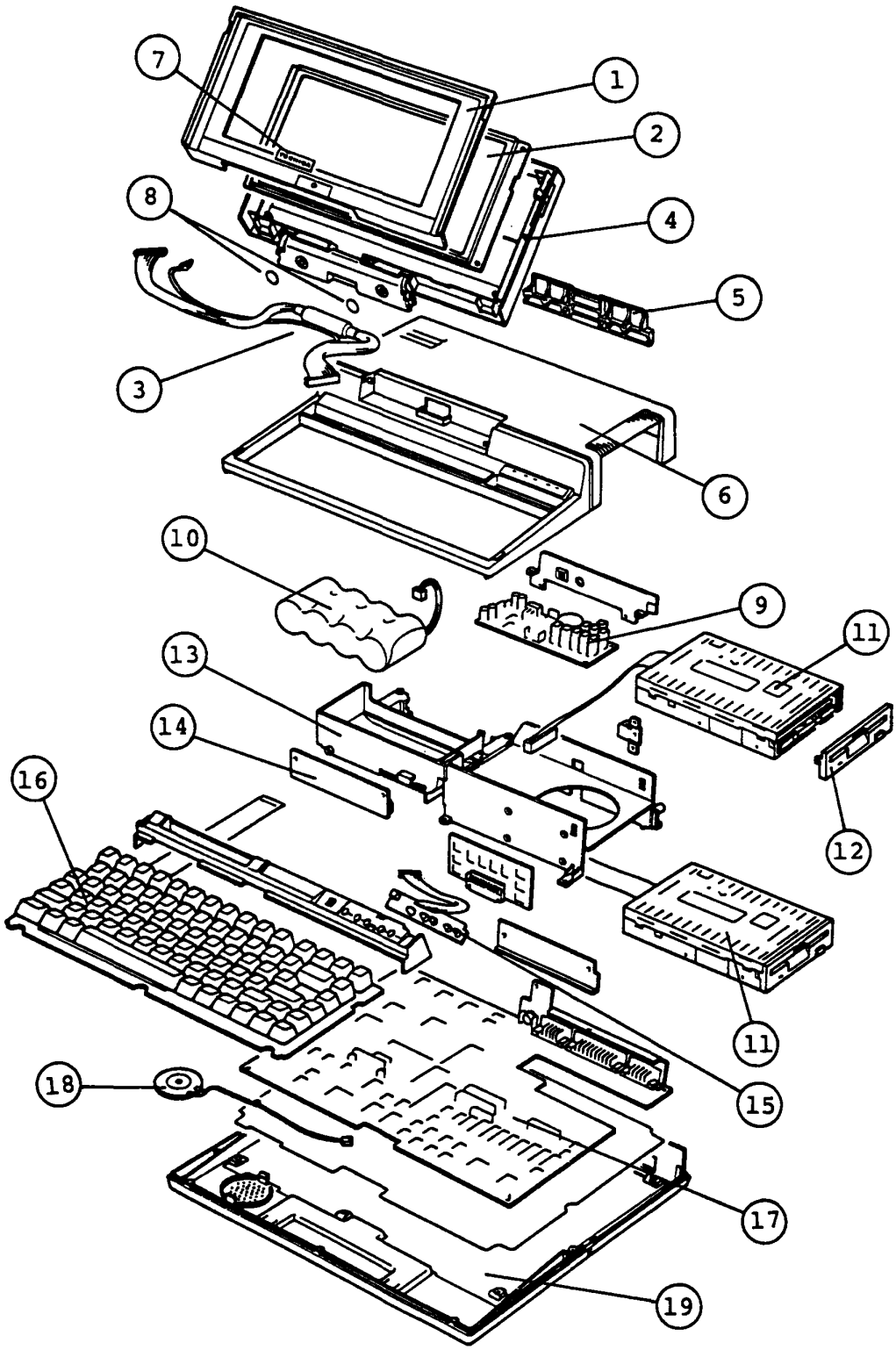
Figure 6-14 System Unit Rear Panel

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
PJ 13		**PJ 14**			
1	GND	1	STROB0	21	GND
2	GND	2	PD01	22	GND
3	CRV1	3	PD11	23	GND
4	CGV1	4	PD21	24	GND
5	CBV1	5	PD31	25	GND
6	CIV1	6	PD41		
7	NC	7	PD51		
8	CHSY1	8	PD61		
9	CVSY1	9	PD71		
		10	ACK0		
		11	BUSY1	**PJ 15**	
		12	PE1	1	DSD1
		13	SELEC1	2	RD0
		14	AUTFD0	3	SD0
PJ 12		15	ERROR0	4	DTR1
1	P26CP	16	PINT0	5	GND
2	GND	17	SLIN0	6	DSR1
		18	GND	7	RTS1
		19	GND	8	CTS1
		20	GND	9	RT1

PART 7 REPLACEMENT PARTS CATALOG

The followings are parts catalogs in accordance with a Field Replaceable Unit (FRU) maintenance philosophy.

7.1 System Unit



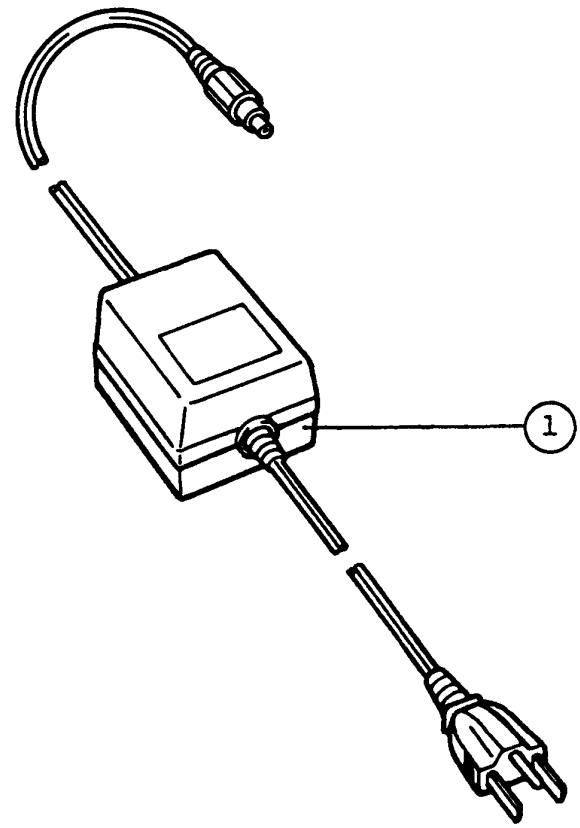
T1100PLUS System

7.1 System Unit (Continued)

INDEX No.	PART NUMBER	DESCRIPTION	NOTE
1	47T108477P1	LCD Mask	
2	VF0014P03	LCD (Liquid Crystal Display)	
3	UL0065P03	LCD Harness	
4	47M140393G1	LCD Cover Sub Assy	
5	47P127400P1	Hinge	
6	47M140394G1	Upper Caver Sub Assy	
7	47K154048P5	Seal 1	
8	47K156063P1	Seal 2	
9	34M741476G01	Power Supply PCB FPLPS1	
10	XZ0075P02	Battery Package	
11	ZA0652P01	3.5" FDD (Floppy Disk Drive)	
12	47M140552G1	FDD Bezel	
13	47T108478P1	FDD Base	
14	34M741481G01	Expansion Slot PCB FPLBP1	
15	34M741486G01	Indicator (LED) PCB FPLED1	
16	UE0182P11 UE0182P12	Keyboard Keyboard	(TEG, TIU) (TAI, TAP)
17	34T779961G01	System Board	
18	39K156042G1	Speaker with Harness	
19	47M140395G1	Lower Cover Sub Assy	

7.2 AC Adaptor

INDEX No.	PART NUMBER	DESCRIPTION	NOTE
1	UA0266P01 UA0266P02	AC Adaptor AC Adaptor	TAI Version TAP Version



AC Adaptor

7.3 5.25" External FDD

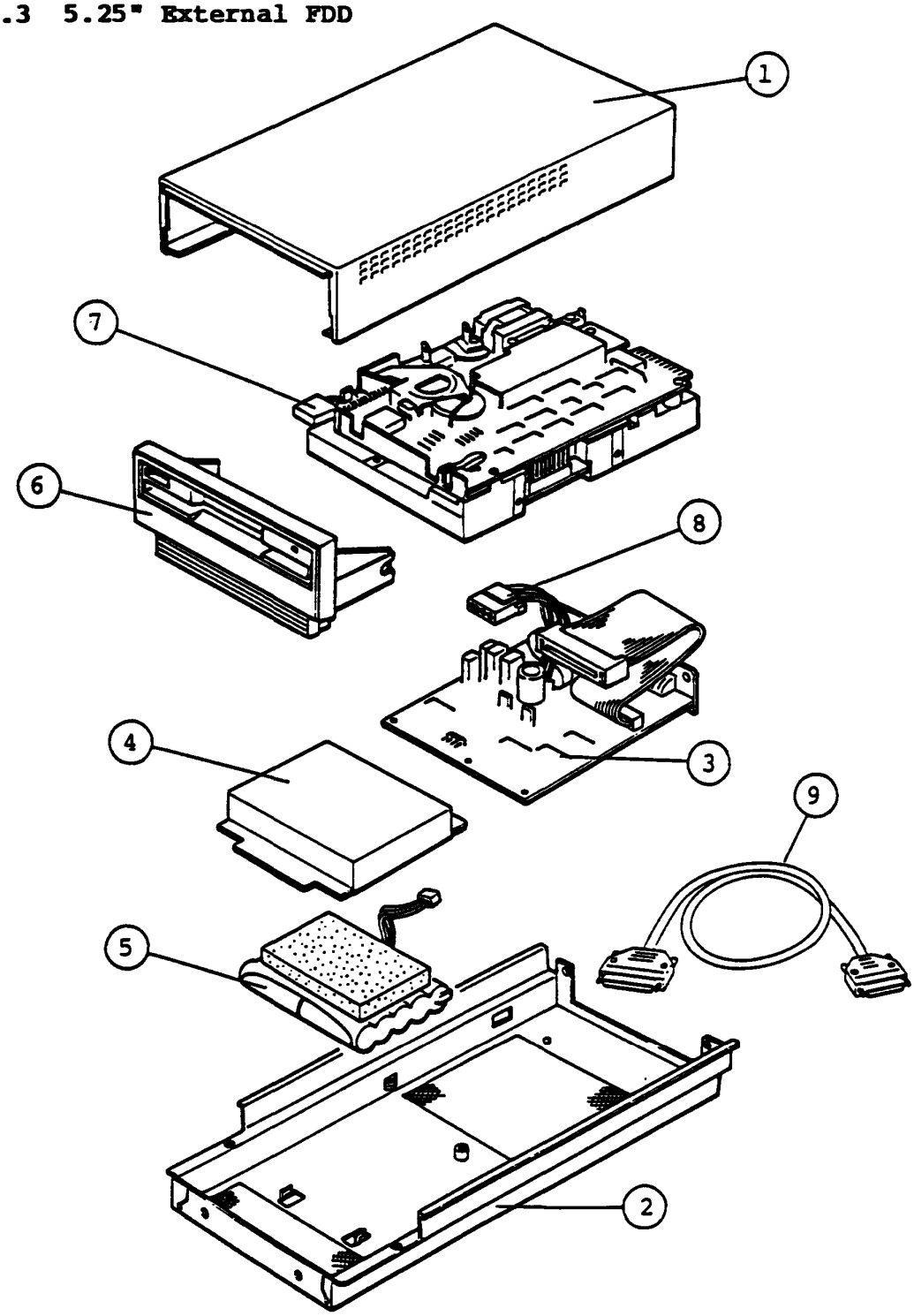


Figure 7-3 5.25" External FDD

7.3 5.25" External FDD (Contiuned)

INDEX No.	PART NUMBER	DESCRIPTION	NOTE
1	47P127086P1	Upper Cover	
2	47P127085P1	Lower Cover	
3	34P710241G01	PCB	
4	47M137924P1	Battery Cover	
5	XZ0067P01	Battery	
6	47P127089P1	Front Panel	
7	ZA0162P01	5.25 inch FDD	
8	UL0034P23	FDD PS Cable	
9	UL0046P13DD004	Cable	

8.1 INTRODUCTION

8.1.1 General

The purpose of this T1100 PLUS Test and Diagnostics is to check the functions of all hardware modules of the T1100 PLUS Personal Computer.

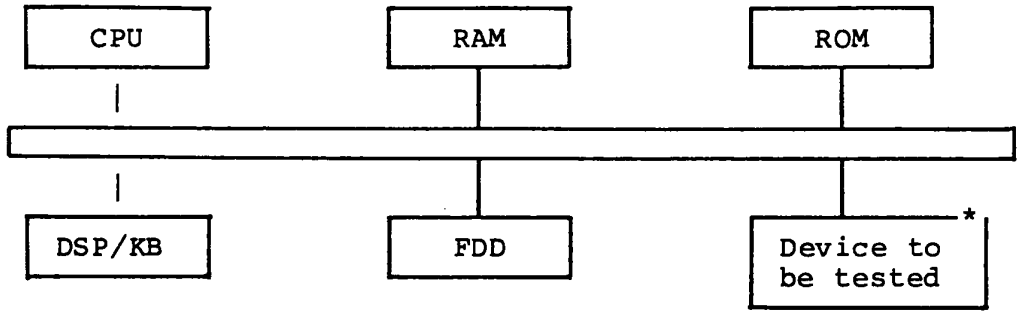
This T1100 PLUS Test and Diagnostics is structured under the MS-DOS, and consists of 17 programs covering all of the hardware modules supported in T1100 PLUS Personal Computer system as described in STRUCTURE section.

The **CE Diagnostic Test Program** is provided as a file in the MS-DOS System Disk. You have to run the MS-DOS before you load the CE Diagnostic Test Program.

The service engineer utilize these programs to isolate the trouble by selecting the appropriate program by the operation procedure described in OPERATION section.

8.1.2 Components Required

The following devices are required to execute the test program system.



Where:

CPU : Central Processer Unit

RAM : Random Access Memory ; 256KB

ROM : Read Only Memory; 32KB

DSP : LCD Unit

KB : Keyboard

FDD : Floppy Disk Drive ;720KB

*
Devices to be tested

RAM : Random Access Memory

ROM : Read Only Memory

KB : Keyboard

DSP : LCD Unit

FDD : Floppy Disk Drive (720KB/360KB)

PRT : Printer Device or Wraparound connector

RSC : Communications controller + Wraparound connector card, Modem

HDD : Hard Disk Drive

RTM : Real Timer

NDP : High speed numeric processor

8.1.3 Structure

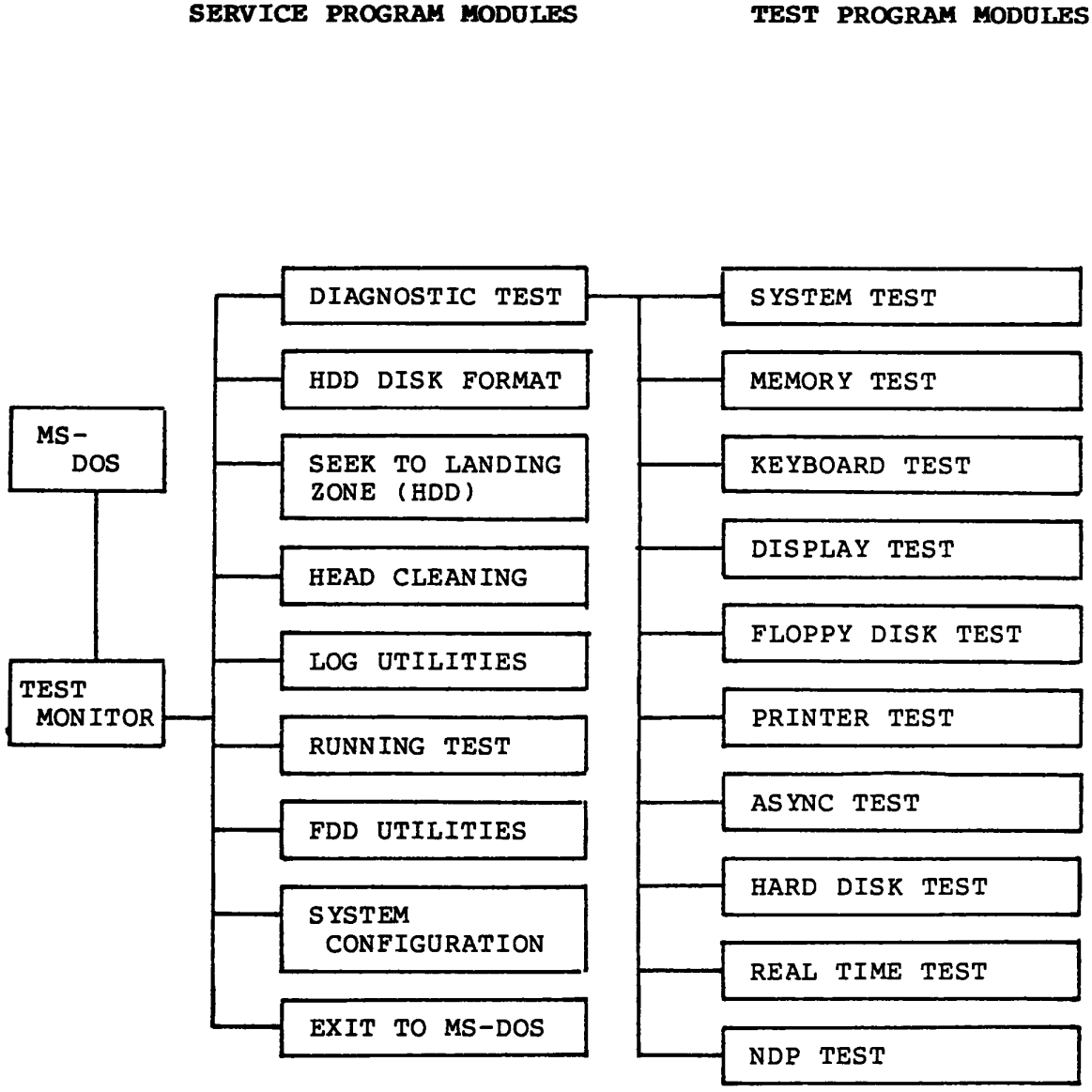
The T1100 PLUS test program system is composed of 17 program modules executed under the Test Monitor.

The 17 program modules can be divided into two groups, the Service Program modules (HDD format, Landing zone seek, Head cleaning, Log utility, Running test, FDD utilities, and System configuration) and the Test Program modules (all other modules). Those are shown in the figure on next page.

Each of the Test Program modules contains some number of subtest programs which are shown in the **ANNEX A:** Test Program List.

Don't execute **NDP Test** .
If you execute NDP Test, error status is displayed on the screen.

TEST PROGRAM STRUCTURE



8.2 OPERATION

This section describes how to operate the T1100 PLUS Test and Diagnostics such as **CE Diagnostic Test Program** . These Diagnostic Test Programs are provided in the MS-DOS System Disk. You have to run the MS-DOS before you load the CE Diagnostic Test Program.

8.2.1 CE DIAGNOSTIC

(1) Test program loading

Insert the MS-DOS disk to the internal disk drive, then turn ON the power of the T1100 PLUS. The MS-DOS is loaded after **Power On Self-test** execution. After the loading, following messages appear on the screen.
And press the "ENTER" Key twice, and then file name of **CE Diagnostic** as **testce** to load the diagnostic program.
If **Current date** and **Current time** is mistake, input the **Enter new date** and **Enter new time** then file name of **Diagnostic** as **testce** to load the diagnostic program.

```
Toshiba Personal Computer (R2100EN)      Preliminary version

Copyright 1984,86 Toshiba Corporation

MS-DOS   Ver 2.11
Copyright 1983,84 Microsoft Corp.

Command  Ver 2.11V
Current date is  Wed  1-01-1986
Enter new date :
Current time is   0:36:46.00
Enter new time :

A>testce
```

The underlined portion on the above screen is for the input message.
After the above operation, the test program loading is complete.

(2)Module selection

The following screen (Diagnostic Menu) is displayed after the test program loading.

```
The TOSHIBA personal computer DIAGNOSTICS
version 0.12 (c) copyright TOSHIBA Corp 1986

DIAGNOSTICS MENU :

  1 - DIAGNOSTIC TEST
  2 - HARD DISK FORMAT
  3 - SEEK TO LANDING ZONE (HDD)
  4 - HEAD CLEANING
  5 - LOG UTILITIES
  6 - RUNNING  TEST
  7 - FDD UTILITIES
  8 - SYSTEM CONFIGURATION
  9 - EXIT TO MS-DOS




 PRESS [1]-[9] KEY
```

Input a module number and then press the "ENTER" key to select the module on DIAGNOSTIC MENU. When you input;

1 : Displays the Diagnostic Test Menu. See page 8-10. (includes pressing "ENTER" key only)
2 : Executes the Hard Disk Format. See page 8-35.

3 : Seeks the head of HDD to Landing Zone. See page 8-37.
4 : Cleans the head of FDD. See page 8-38.

5 : Displays the error logs. See page 8-39.

6 : Executes the running test. See page 8-41.

7 : Executes the format, copy and dump of FDD. See page 8-42.
8 : Displays the system configuration. See page 8-43.

9 : Returns to MS-DOS

If you input the except above module number, the screen return to the Diagnostic Menu. (above screen)

(3) Displaying of system configuration

After press "8" and "ENTER" keys of DIAGNOSTIC MENU, the following system configuration is displayed on the LCD Unit/CRT Display Unit.

```
SYSTEM CONFIGURATION :

  * - 640KB MEMORY

  * - LCD DISPLAY

  * - 2 FLOPPY DISK DRIVE(S)

  * - 1 ASYNC  ADAPTER

  * - 0 HARD DISK DRIVE(S)

  * - 1 PRINTER ADAPTER

  * - 0 MATH CO-PROCESSOR



PRESS [ENTER] KEY
```

Above message is an example of F/F type System .

Compare your System Unit and System Configuration of above message, and then if it is good, press the "ENTER" key.
If it is no good, turn OFF the power switch of the System Unit, and then check the configuration DIP switch. (Refer to page 1-10)
Repeat the operation from step (1) after correcting them.

(4) Test selection

After press "1" and "ENTER" keys of DIAGNOSTIC MENU, the following screen appears on the LCD Unit/CRT Display Unit.

```
The TOSHIBA personal computer DIAGNOSTICS
version 0.12 (c) copyright TOSHIBA Corp 1986

DIAGNOSTIC TEST MENU :

   1 - SYSTEM TEST
   2 - MEMORY TEST
   3 - KEYBOARD TEST
   4 - DISPLAY TEST
   5 - FLOPPY DISK TEST
   6 - PRINTER TEST
   7 - ASYNC TEST
   8 - HARD DISK TEST
   9 - REAL TIMER TEST
  10 - NDP TEST
  88 - FDD & HDD ERROR RETRY COUNT SET
  99 - EXIT TO DIAGNOSTICS MENU



PRESS [0]-[9] KEY
```

Input the test number, and then press the "ENTER" key to execute the DIAGNOSTIC TEST MENU.

If you input the above test number (1 - 10), System Unit execute the each test.

If you input the above test number (88), You can set the error retry count of the FDD and HDD.

If you input the above test number (99), the Screen return to the DIAGNOSTIC MENU. (Refer to page 8-8.)

If you input except above test number, the screen return to the Diagnostic Test Menu. (above screen)

(5) Subtest and test mode selection

The subtest menu screen (the following sample is for FDD) is displayed after selecting any test(1-7) at test selection, so input two digit subtest number.
(Refer to **ANNEX A:** Test Program List)

```
FLOPPY DISK                                    501000


SUB-TEST   : 01
PASS COUNT: 00000      ERROR COUNT: 00000
WRITE DATA: 00         READ  DATA : 00
ADDRESS    : 000000    STATUS     : 000

SUB-TEST MENU :

01 - Sequential read
02 - Sequential read/write
03 - Random address/data
04 - Write specified address
05 - Read specified address
99 - Exit to DIAGNOSTIC TEST MENU



SELECT SUB-TEST NUMBER  ? 01
TEST  LOOP (1:YES/2:NO) ? 2
ERROR STOP (1:YES/2:NO) ? 1
```

where,

TSSDSS

- Status (Refer to **ANNEX C**)
- Device number
- Subtest number (Refer to **ANNEX A**)
- Test number (Refer to **ANNEX A**)

Note 1 : Subtest number

Select a subtest by typing two-digit number. The input number "99" make the control return to Diagnostic Test Menu.

Note 2 : Test mode selection

The test program execution mode can be specified as follows after the test ends or when an error occurs.

TEST LOOP (1:YES/2:NO) ?

1 : At each time a test cycle ends, it increments the pass counter by one and repeats the test cycle. (If you press "RETURN" key, it is assumed to be TEST LOOP 1:YES.)

2 : At the end of test cycle, it terminates the test execution and exits to the subtest selection menu.

ERROR STOP (1:YES/2:NO) ?

1 : When an error occurs, it displays the error status at column 7 (Refer to **ANNEX C**) and stops the execution of test program. The operation guide displays on the right side of the screen as follows.

```
((HALT OPERATION))
  1 : Test End
  2 : Continue
  3 : Retry
```

Input "1" key : It terminates the test program execution and exits to the subtest selection menu.
Input "2" key : It continues the test.
Input "3" key : It retrys the test.

2 : When an error occurs, it displays the error status, then it increments the error counter by one and goes to the next test step.

Note : The Running test will neglect the "TEST LOOP (N)", and "ERROR STOP (Y)".
If you stop the Running test, press "Ctrl" + "Break" keys. The screen return to the DIAGNOSTIC MENU.

(6) Termination

When it is needed to terminate the test program execution, press the **"Ctrl" + "Break"** keys. The screen return to the DIAGNOSTIC MENU.

8.3 SYSTEM TEST

Summary of the System Test

This program performs the checksum test of the ROM on the Systems PCB. (Test limits : F8000H - FFFFFH, 32KB)

Subtest and test mode selection

After pressing "1" and "ENTER" keys at test selection of DIAGNOSTIC TEST MENU, the following screen appears for subtest and test mode selection.

```
SYSTEM TEST                                  XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - ROM checksum
02 - Secound ROM checksum
99 - Exit to DIAGNOSTIC TEST MENU









SELECT SUB-TEST NUMBER  ?
```

Select desired subtest by pressing two digits subtest number in SUBTEST MENU as shown above and "ENTER". Then select the test mode by pressing "1:YES" or "2:NO" and "ENTER" keys for **TEST LOOP** and **ERROR STOP** question respectively.

The selected subtest starts and test information such as **SUBTEST No., PASS COUNT, ERROR COUNT, WRITE DATA, READ DATA, ADDRESS** , and **STATUS** are displayed and updated during execution as shown above.

8.4 MEMORY TEST

Summary of the Memory Test

This test performs the memory read/write test with constant data (Five patterns) and address pattern data and also memory refresh test for RAM.

Subtest and test mode selection

After pressing "2" and "ENTER" keys at test selection on the DIAGNOSTIC TEST MENU, the following screen appears for subtest and test mode selection.

```
MEMORY TEST                              XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - RAM constant data
02 - RAM address pattern data
03 - RAM refresh
99 - Exit to DIAGNOSTIC TEST MENU









SELECT SUB-TEST NUMBER  ?
```

Select desired subtest by pressing two digits subtest number in SUBTEST MENU as shown above and "ENTER" key. Then select the test mode by pressing "1:YES" or "2:NO" and "ENTER" for **TEST LOOP** and **ERROR STOP** question respectively.

The selected subtest starts and test information such as **SUBTEST No., PASS COUNT, ERROR COUNT, WRITE DATA, READ DATA, ADDRESS,** and **STATUS** are displayed and updated during execution as shown above.

Refer the following page for subtest description.
Refer to the **ANNEX C** for error status code.

Subtest description

(Test limits : 0H - Max size)

Subtest 01 Constant data read/write test

Writes constant data to Memory, and then reads and compares it with the original data.
The constant data are "FFFFH", "AAAAH", "5555H", "0101H" and "0000H".

Subtest 02 Address pattern data read/write test

Makes the segment address and offset address by XORing, and then writes the address pattern data it and reads and compares them with a original data.

Subtest 03 Memory refresh test

Writes constant data in 256 byte length to Memory, and then reads and compares it with the original data. The constant data are "AAAAH" and "5555H".
A certain interval time will be taken between the write and the read operations.

8.5 KEYBOARD TEST

Summary of the Keyboard Test

This test performs the function test of keyboard by pressing all the keys according to the keyboard pattern on the screen.

Subtest and test mode selection

After pressing "3" and "ENTER" keys at test selection of DIAGNOSTIC TEST MENU, the following screen appears for subtest and test mode selection.

```
KEYBOARD TEST                              XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - Pressed key display
99 - Exit to DIAGNOSTIC TEST MENU









SELECT SUB-TEST NUMBER  ?
```

Select desired subtest by pressing two digits subtest number in SUBTEST MENU as shown above and "ENTER" key. Then select the test mode by pressing "1:YES" or "2:NO" and "ENTER" keys for **TEST LOOP** and **ERROR STOP** question respectively.

The selected subtest starts and test information such as **SUBTEST No., PASS COUNT, ERROR COUNT, WRITE DATA, READ DATA, ADDRESS,** and **STATUS** are displayed and updated during execution as shown above.

Refer the following page for subtest description.
Refer to the **ANNEX C** for error status code.

Subtest description

Keyboard layout is drawn on the Display, and when a certain key is pressed, the character "*" will be displayed at the corresponding location of the screen.

If the same key is pressed again, it becomes to be the original state so that it is able to confirm the self-repeat function.

If you stop the Keyboard test, press "Ctrl" + "Break" keys.

Note: If state of **Num Lock** is ON, you can not execute exact test.

8.6 DISPLAY TEST

Summary of the Display Test

This test performs the test of VIDEO RAM read/write, attribute character, character mode display, graphic mode display, and screen page for LCD and its controller function.

Subtest and test mode selection

After pressing "4" and "ENTER" keys at test selection of DIAGNOSTIC TEST MENU, the following screen appears for subtest and test mode selection.

```
DISPLAY TEST                              XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - VRAM read/write
02 - Character attributes
03 - Character set
04 - 80 * 25 Character display
05 - Graphics display (color set 0/1)
06 - 640 * 200 Graphics display
07 - 640 * 400 Graphics display
08 - Display page
09 - "H" pattern display
99 - Exit to DIAGNOSTIC TEST MENU


SELECT SUB-TEST NUMBER  ?
```

Select desired subtest by pressing two digits subtest number in **SUBTEST MENU** as show above and "ENTER" key. Then select the test mode by pressing "1:YES" or "2:NO" and "ENTER" for **TEST LOOP** and **ERROR STOP** question respectively.

The selected subtest starts and test information such as **SUBTEST No., PASS COUNT, ERROR COUNT, WRITE DATA, READ DATA, ADDRESS,** and **STATUS** are displayed and updated during execution as shown above.

Refer the following page for subtest description.
Refer to the **ANNEX C** for error status code.

Subtest description

Subtest 01 Read/write test of video RAM

In the display-off mode, it writes the constant data such as "FFH", "AAH", "55H", "00H" to the video RAM, then it reads and compares them with the original data.

Subtest 02 Character attribute display test

Normal Display
Intensified Display
Reverse Display
Blinking Display

* Note : If it is a color CRT display unit, you checks background color, foreground color, border color about each of seven colors of blue, green cyan, red magenta, yellow and white.

Subtest 03 Display of character set

Displays in 40 x 25 Test mode character codes "00H" though "FFH".

Subtest 04 Display of 80 x 25 characters

Displays Shift-Characters.

Subtest 05 In the case of Color Display:

Displays three painted blocks with color set 0 in 320 x 200 graphic mode.

Blocks color green, red, and yellow

Displays three painted blocks with color set 0 in 320 x 200 graphic mode.

Blocks color Cyan, magenta, and white.

In the case of Plasma Display:

Screen is lighten in order of RED MAGENTA, GREEN CYAN, YELLOW WHITE.

Subtest 06 Display in 640 x 200 graphic mode

It displays in the screen Black & white.

Subtest 07 It cann't executes.

To be continued.

Subtest description (Continued)

Subtest 08 Screen Page test

Displays the contents of VIDEO RAM to the CRT in 40 x 25 test mode. VIDEO RAM contains a capacity of 8 screen pages and each screen page is displayed as all "0", all "1" .... and all "7" respectively.

Subtest 09 "H" Pattern display test

Display of "H" character on the whole screen.

8.7 FLOPPY DISK TEST

Summary of the FLOPPY DISK Test

This test performs the read/write test with sequencial address, random address, and specified address for FDD and its controller functions.

Subtest and test mode selection

After pressing "5" and "ENTER" keys at test selection of DIAGNOSTIC TEST MENU, the following message appear on the screen.

Test drive number select (1: FDD1, 2: FDD2, 0: FDD1&2) ?

1: Executes only FDD1 test.

2: Executes only FDD2 test.

0: Executes FDD1 and FDD2 test.

After you choose the drive number of FDD, then input it.

To be continued.

Subtest and test mode selection (Continued)

The following screen appears for subtest and test mode selection.

```
FLOPPY DISK                              XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - Sequential read
02 - Sequential read/write
03 - Random address/data
04 - Write specified address
05 - Read specified address
99 - Exit to DIAGNOSTIC TEST MENU




SELECT SUB-TEST NUMBER  ?
```

Select desired subtest by pressing two digits subtest number in SUBTEST MENU as shown above and "ENTER" key. Then select the test mode by pressing "1:YES" or "2:NO" and "ENTER" keys for **TEST LOOP** and **ERROR STOP** question respectively.

The selected subtest starts and test information such as **SUBTEST No., PASS COUNT, ERROR COUNT, WRITE DATA, READ DATA, ADDRESS** ,and **STATUS** are displayed and updated during execution as shown above.

Refer the following subtest description.
Refer to the **ANNEX C** for error status code.

Subtest description

Subtest 01 Sequential read test

Reads all tracks sequencially and checks CRC.

Subtest 02 Sequential read/write test

Writes data to all tracks sequencially, and then reads the data back and compares them with the original data.
(The data pattern,"B5ADAD H", is repeated.)

Subtest 03 Random address/data read/write

Writes random data into tracks gelected at random, and then reads the data back and compares them with the original data.

Subtest 04 Specified address write test

Writes the data into a track and a head specified and head address done through the Keyboard.

Subtest 05 Specified address read test

Reads the data from the track and head address specified through the Keyboard.

Note: Use one of the following "Format" programs to format a work disk according to the disk type.
In the case of 2D(FORMAT /4), formatted tracks are 0 thru 39.
In the case of 2DD(FORMAT), formatted tracks are 0 thru 79.

8.8 PRINTER TEST

Summary of the Printer Test

This test performs the test of ripple pattern, functions(six print modes), and wraparound for printer and its controller.

Subtest and test mode selection

After pressing "6" and "ENTER" keys at test selection of DIAGNOSTIC TEST MENU, the following screen appears for subtest and test mode selection.

```
PRINTER TEST                              XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - Ripple pattern
02 - Function
03 - Wrap around
99 - Exit to DIAGNOSTIC TEST MENU




 SELECT SUB-TEST NUMBER  ?
```

Select desired subtest by pressing two digits subtest number in SUBTEST MENU as shown above and "ENTER" key. Then select the test mode by pressing "1:YES" or "2:NO" and "ENTER" keys for **TEST LOOP** and **ERROR STOP** question respectively.

The selected subtest starts and test information such as **SUBTEST No., PASS COUNT, ERROR COUNT, WRITE DATA, READ DATA, ADDRESS** ,and **STATUS** are displayed and updated during execution as shown above.

Refer the following page for subtest description.
Refer to the **ANNEX C** for error status code.

Subtest description

Subtest 01 Ripple pattern test

Prints characters (codes "20H" through "7EH") on a line rotating the line pattern by one character to the down lines.

Subtest 02 Function test

Normal Print
Double Width Print
Compressed Print
Emphasized Print
Double Strike Print
All Characters Print

Subtest 03 Wraparound test

Checks the data, control, and status lines with the Printer Wraparound Connector(Part No.).

Note: Subtest 01 and subtest 02 needs the channel selection.

8.9 ASYNC(RS232C) TEST

Summary of the ASYNC(RS232C) Test

This test performs the data transmission(Send/Receive) with the CCM Wraparound Connector(Part No.).

Subtest and test mode selection

After pressing "7" and "ENTER" at test selection, the following screen appears for subtest and test mode selection.

```
ASYNC TEST                                  XXXXXXX.


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - Wrap around (channel-1)
02 - Wrap around (channel-2)
03 - Point to point (send)
04 - Point to point (receive)
05 - Card modem loopback
06 - Card modem on-line test
07 - Dial tester test
99 - Exit to DIAGNOSTIC TEST MENU


SELECT SUB-TEST NUMBER  ?
```

[illegible] in SUBTEST MENU as shown above and "ENTER" key. Then select the test mode by pressing "1:YES" or "2:NO" and "ENTER" keys for **TEST LOOP** and **ERROR STOP** question respectively.

The selected subtest starts and test information such as **SUBTEST No., PASS COUNT, ERROR COUNT, WRITE DATA, READ DATA, ADDRESS,** and **STATUS** are displayed and updated during execution as shown above.

Refer the following page for subtest description.
Refer to the **ANNEX C** for error status code.

Subtest description

Note: Communication mode of subtest 01 - 05 is as follows;
Async, 9600 BPS, 8 data bit + parity (even), 1 step bit, data = 20H - 7EH.
From subtest 03 to subtest 07 need the channel selection.

Subtest 01 Wrap around test (channel - 1)

Performs a data send/receive test with the wraparound connector for the channel 1.

Subtest 02 Wrap around test (channel - 2)

Performs the same test as subtest 01 for the channel 2.

Subtest 03 Point to point test (send)

Sends data (codes 20H through 7EH) to another communication device referred to as a receiver, and receive the data from the receiven, then compared them with original data.

Subtest 04 Point to point test (receive)

Receives the data from another communication device (referred to as a transmitter) comparesthem with original data then back the data to the transmitter.
Note: Subtest 03 (send side) and subtest 04 (receive side) is pare.

Subtest 05 Card modem loopback test

Sends data to a card modem, then receives the data looped back in the card modem, then compares them with original data.

Subtest 06 Card modem on-line test

Sends data to a card modem through data a PBX, then receive looped back and compares them with original data.
Communication mode is 110/300/1200 BPS, 8 data bits + no parity, 1 stop bit, data = 20H - 7EH codes.

To be continued.

Subtest 07 Dial tester test

Performs pules dial and tone dial test with a dial tester.
The pulse dial test sends the pulse "1-2-3-4-5-6-7-8-9-0-1-2" twice.
The tone dial send the data "1-2-3-4-5-6-7-8-9-*-0-#" twice.

8.10 HARD DISK TEST

Summary of the HARD DISK Test

WARNING

The data on the HDD will be lost permanenty during the write operations in subtests 2, 3, 4, 6 and 8.

Current disk contents will be completely destroyed. Save the data on Hard Disk before execute this program if you don't want to do so.

If you execute the subtest 2, 3, 4, 6 and 8 must set the partition of HDD. (Refer to 8.20 Set the partition)

This test performs the read/write test with sequential address, randam address, and specified address and so on for HDD and its controller function.

To be continued.

Subtest and test mode selection

After pressing "8" and "ENTER" keys appear the following message on the screen.

Test drive number select (1: HDD1, 2: HDD2, 0: HDD1&2) ?

1: Executes the test of only drive 1.
2: Executes the test of only drive 2.
3: Executes the test of drive 1 and drive 2.

After you choose the above number, then press it.
The following screen appears on the display for subtest selection.

```
HARD DISK TEST                              XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX      ERROR COUNT: XXXXX
WRITE DATA: XX         READ  DATA : XX
ADDRESS    : XXXXXX    STATUS     : XXX

SUB-TEST MENU :

01 - Sequential read
02 - Address uniquence
03 - Random address/data
04 - Cross talk & peek shift
05 - Write/read/compare(CE)
06 - Write specified address
07 - Read  specified address
08 - ECC circuit (CE cylinder)
99 - Exit to DIAGNOSTIC TEST MENU



SELECT SUB-TEST NUMBER  ?
```

Selected desired subtest by pressing two digits subtest number in **SUBTEST MENU** as shown above and "ENTER" key. Then select the test mode by pressing "1:YES" or "2:NO" and "ENTER" keys for **TEST LOOP** and **ERROR STOP** question respectively.

The selected subtest starts and test information such as **SUBTEST No., PASS COUNT, ERROR COUNT, WRITE DATA, READ DATA, ADDRESS,** and **STATUS** are displayed and updated during execution as shown above.

Refer to the **ANNEX C** for error status code.

Subtest description

Subtest 01 Sequential read test(CYL.0-610,CYL.610-0)

Performs the Forword Read(0-610 tracks) and Reverse Read(610-0 tracks).

Subtest 02 Address uniquence test

Writes the address data(sector by sector) track by track, then reads the data and compare them. Following three kind of reads operations are performed.
(Forward sequential, Reverse sequential, Randam)

Subtest 03 Randam address/data test

Write, read and compare the data at randam address (Cyl, Head, and Sec) and randam length.

Subtest 04 Cross talk & peek shift test

Write, read and compare the worst pattern data (8types such as B5ADADH, 4A5252H, EB6DB6H, 149249H, 63B63BH, 9C49C4H, 2DB6DBH, and D24924H) cylinder by cylinder to check the interference between the tracks.

Subtest 05 CE cylinder(611) Write/Read/Compare test

The Worst pattern data (B5ADADH) is used in this test.

Subtest 06 Specified address write test

Writes the data at the specified cylinder and head address.

Subtest 07 Specified address read test

Read the data at the specified cylinder and head address.

Subtest 08 ECC circuit test

Checks the ECC circuit functions at CE cylinder (611 cylinder).

8.11 REAL TIMER TEST

Summary of the REAL TIME test

This test performs the check test of the calender and timer.

Subtest and test mode selection

After pressing "9" and "ENTER" keys at test selection of DIAGNOSTIC TEST MENU, the following screen appears for subtest and test mode selection.

```
REAL TIME TEST                              XXXXXXX


SUB-TEST   : XX
PASS COUNT: XXXXX       ERROR COUNT: XXXXX
WRITE DATA: XX          READ  DATA  : XX
ADDRESS    : XXXXXX     STATUS      : XXX

SUB-TEST MENU :

01 - Real time test
02 - Real time carry set
99 - Exit to DIAGNOSTC TEST MENU




SELECT SUB-TEST NUMBER  ?
```

Select desired subtest by pressing two dights subtest number in SUBTEST MENU as shown above and "ENTER".

Subtest description

Subtest 01 Real time test

The Current date and time are display, and new date and new time are possible to be entered.

Subtest 02 Real timer set

WARNING : If this test execute, Current date and Current time return to "12-31-1985" "23:59:55".

Confirm that up date Current date and time are displayed on the screen.
Start the from the menu as follow.

Current date : 12-31-1985

Current time : 23:59:55

8.12 NDP (8087) TEST

You can't execute this test.
If you execute this test, error status is displayed on the screen.

8.13 HARD DISK FORMAT

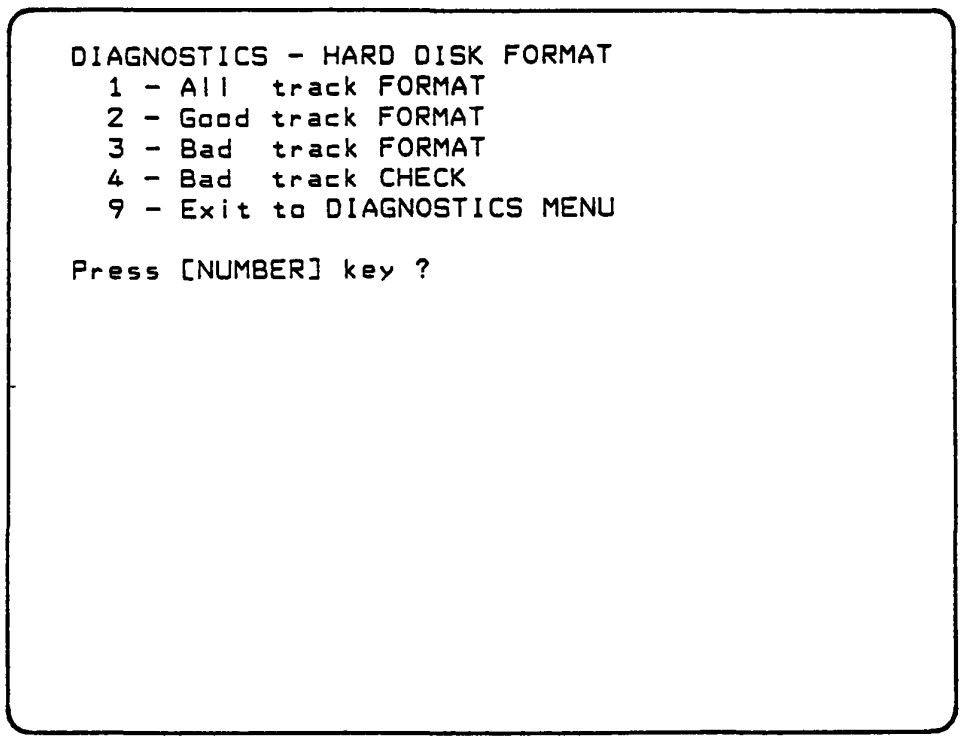
Summary of the program

WARNING : Current disk contents will be completely destroyed. Save the data on Hard Disks before execute this program if you don't want yo do so.

If Formats a Hard Disk Drive with the specified format and 4 types operation described in program description on next page.

Program execution

After pressing "2" and "ENTER" keys at task selection of **DIAGNOSTIC MENU** , the following screen appears before execution.



To be continued.

Program description

(1) All track FORMAT (Execution time 6 minutes)

Executes format of Hard Disk.

Secter sequence	:	3
Cylinder	:	612 (0 - 611)
Head	:	2 (0 - 1)
Sector	:	17 (1 - 17)
Sector length	:	512 Byte/sector
Bad track	:	Up to 12 tracks (If more than track were typed-in, the program is terminated.)

All track format execute as follws.

1. Reads the all track, and then check the Bad track information now.
2. You input the Bad track information.
3. Formats the all track by Good track format.
4. Writes the Bad track by information of 1 and 2.
5. Executes Read test to all track, and error track dicide the Bad track.

(2) Good track FORMAT (Execution time 1 second)

Executes the format of appointed cylinder and track as good-track.

(3) Gad track FORMAT (Execution time 1 second)

Executes the format of appointed cylinder and track as bad-track.

(4) Bad track CHECK (Execution time 1 and half minutes)

Check for the bad-track by read operation about all-track on the Hard Disk, then it display list of bad-track.

8.14 SEEK TO LANDING ZONE

Summarry of the program

This program moves head of the Hard Disk Drive to Landing Zone.

Note: When it does not issues any command to HDD for 5 seconds, heads of the Hard Disk Drive moves to Landing zone antomatically.

8.15 HEAD CLEANING

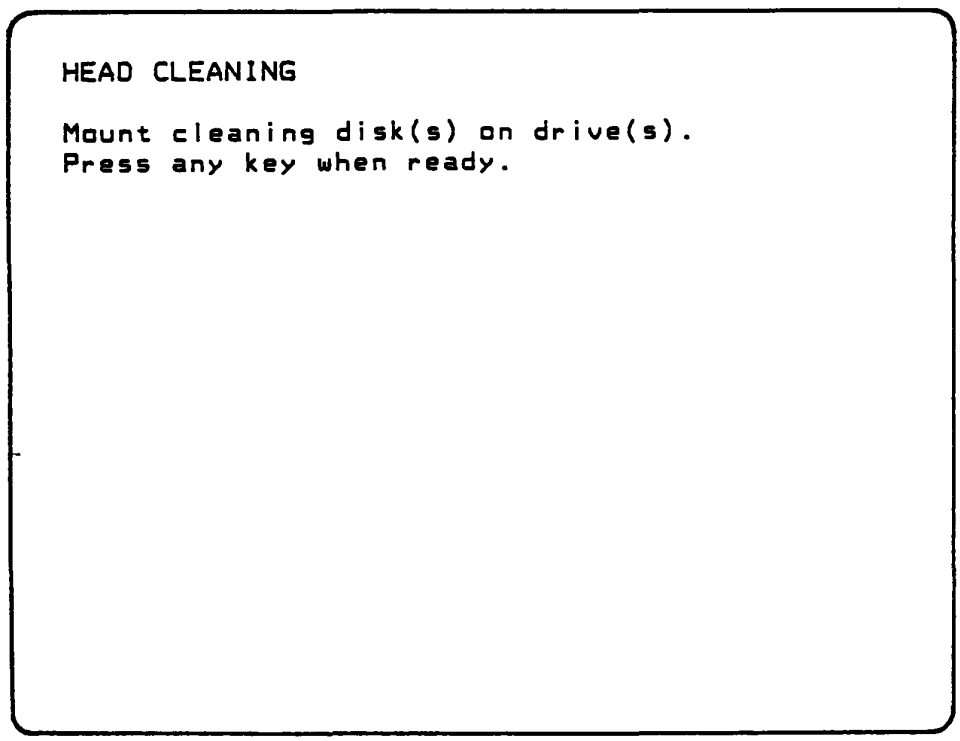
Summary of the program

It executes the head load, seek and read operation for the purpose of head cleaning.

The Cleaning Disk Kit(Part No.) is required to perform the cleaning properly.

Program execution

After pressing "4" and "ENTER" at task selection of **DIAGNOSTIC MENU** , the following screen appears before test execution.



After the above message apper on the screen, then set the Cleaning Disk to FDD and press the any key.

The message of **"Cleaning start"** is displayed on the screen and Head Cleaning is executed.

When it is finished, it return to the **Diagnostic Menu** .

8.16 LOG UTILITES

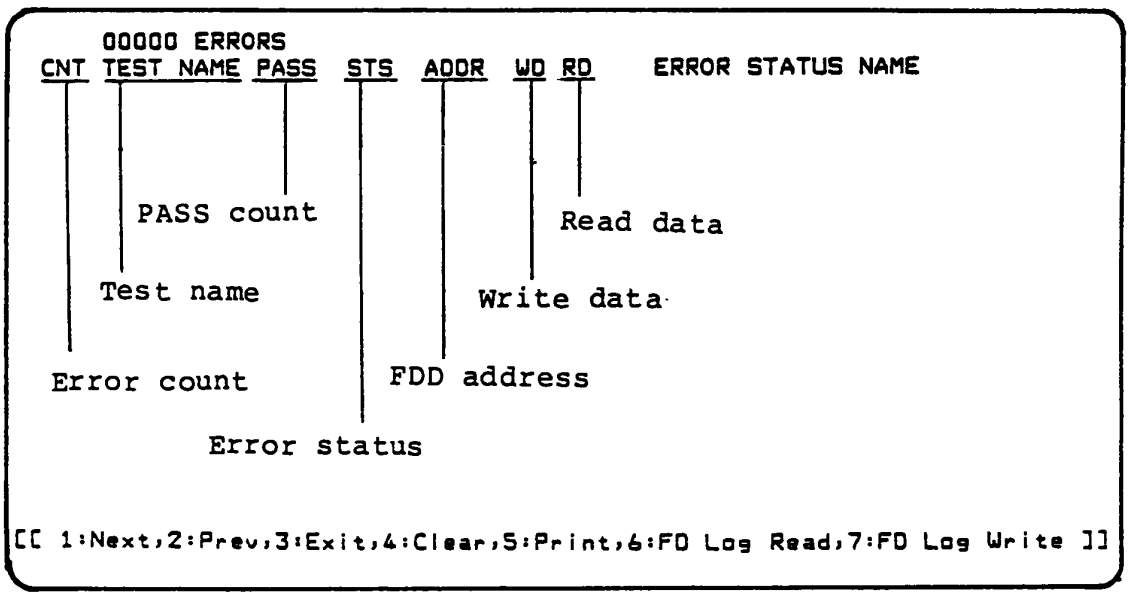
Summary of the program

The error information detected while testing is logged in the memory or the test floppy disk.
The logged error information is able to be displayed on the CRT or be printed out through the printer.

Program execution

The error information logged in the Memory or the floppy disk is displayed as shown below by press "5" key during the task selecting operation.

Error Display



Operation guide is displayed bottom of the screen.
Error status name is displayed right side of the screen.

The following functional keys are available for the error display screen.

"1" key : One page is scrolled upwards.

"2" key : One page is scrolled downwards.

"3" key : It returns to task selection.

"4" key : All error logs in RAM are erased.

To be continued.

"5" key : The error logs are printed out through the printer.

"6" key : The error logs in floppy disk are displayed on the CRT.

"7" key : The error logs in RAM are written to floppy disk.

Note : When the error retry was made successfully, the "R" character is added at the head of error status.
In this case, the error count is not updated.

8.17 RUNNING TEST

Summary of the program

The Running Test makes a sequential and continuous execution of the test programs specified by the test list of system parameter with taking no man's intervention. Under the execution of Running Test, it displays the test name and subtest number being currently executed.

Program execution

Prior to the execution of Running test, the screen shows the following messages asking of execution or non-execution of printer and ASYNC wraparound test, and display selection .

(1) **Printer wraparound test (1:YES/2:NO)?**

1 : It executes the printer wraparound test.

2 : It does not execute the printer wraparound test.

(2) **Async wraparound test (1:YES/2:NO)?**

1 : It executes the async wraparound test.

2 : It does not execute the async wraparonud test.

The Running Test executes the following test programs

Test name to be tested		Subtest number in sequential execution
1. System	:	01
2. Memory	:	01, 02, 03, 04
3. Display	:	01 - 08
* 4. FDD	:	02
5. Printer	:	03 (Printer Wraparound Connector Part No. is required.)
6. RS232C	:	01 (CCM Wraparound Connector Part No. is required.)

Refer to **ANNEX A** , Test Program List, for summary of the subtests or Subtest description in each program module for the details.

(* mark : Automatically select "1"(one FDD) or "0"(two FDD.)

8.18 FDD UTILITES

(1) FORMAT

Formats a Floppy Disk
Two-sided doble density double-track, 48TPI,MFM mode
512 Byte, 9 sectors/track (2D)
Two-sided doble density double-track, 96TPI, MFM mode
512 Byte, 9 sector/track (2DD)

(2) COPY

Copys a Floppy Disk
Copy with one FDD (Drive A)
Copy with two FDDs (from drive A to B)

(3) DUMP

Displays contents of Floppy Disk (each type) or Hard Disk (designated sector).

8.19 SYSTEM CONFIGURATION

Summary of the program

It displays your system's configuration such as Memory size, Display type, Number of FDD(s), Number of HDD, Number of RS232C, Number of Printer and option.

```
SYSTEM CONFIGURATION :

  * - 640KB MEMORY
  * - LCD DISPLAY
  * - 2 FLOPPY DISK DRIVE(S)
  * - 1 ASYNC ADAPTER
  * - 0 HARD DISK DRIVE(S)
  * - 1 PRINTER ADAPTER
  * - 0 MATH CO-PROCESSOR



PRESS [ENTER] KEY
```

Above message is an example of F/F type System.

8.20 SET THE PARTITION

Summary of the program

This program set the partition of Hard Disk.

In the case of following items, you need to set the partition of Hard Disk.

1. Replacing the good spare HDD.
   Note: After formating the HDD, executes it.
   (Refer to paragraph 8.12)

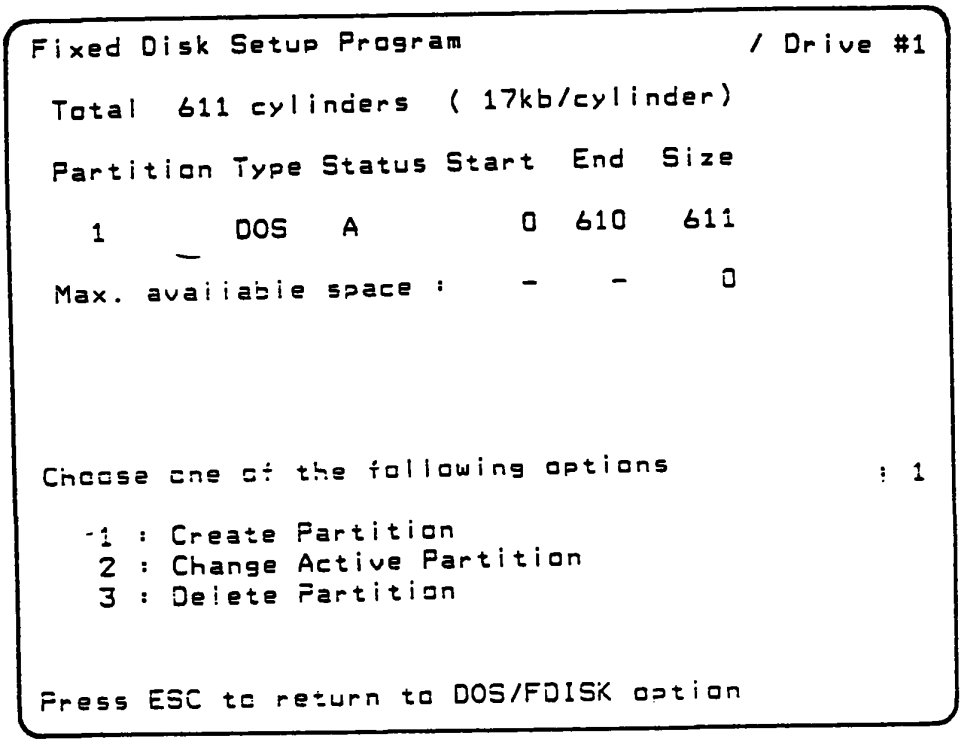
2. Breaking the media of HDD.

3. Executing the Hard Disk Test of Test & Diagnostic.

To be continued.

Program execution

Insert the MS-DOS System Disk into the internal disk drive, then turn on the power of the T1100 PLUS System.
After MS-DOS loading, press the "ENTER" key twice.
INPUT **"FDISK"** then press "ENTER" keys, then the following screen appears for the partiton setting.



1: Executes partition setting

2: Changes the strat address and end address of the partition.

3: Deletes the partition setting.

Refer to OWNER"S MANUAL.

ANNEX A : TEST PROGRAM LIST

TEST No.	TEST NAME	SUBTEST No.	TEST ITEM
1	SYSTEM	01	ROM Checksum
2	MEMORY	01 02 03	Constant Data R/W test Address Pattern R/W test Memory Refresh Test
3	KEYBOARD	01	
4	DISPLAY	01 02 03 04 05 06 07 08	Video RAM R/W Test Character Attribute display Character Set display 80 x 25 display 320 x 200 Graphic display 640 x 200 Graphic display 640 x 400 Graphic display Screen Page Test
5	FDD	01 02 03 04 05	Sequential Read Test Sequential R/W Test Random Address/Data R/W Test Specified Address Write Test Specified Address Read Test
6	PRINTER	01 02 03	Ripple Pattern Test Function Test Wraparound Test (It needs wraparound connector.)
7	ASYNC/ (RS232C)	01 02 02 03 04 05 06 07	Wraparound (chanel-1)Test (It needs wraproud connector) Wraparound (chanel-2)Test (It needs wraproud connector) Point to point Test (send) ( ) Point to point Test (recive) ( ) Card modem loopback Test Card modem on-line Test Dial tester Test

ANNEX A : TEST PROGRRAM LIST (Continued)

TEST No.	TEST NAME	SUBTEST No.	TEST ITEM
8	HDD	01 02 03 04 05 06 07 08	Sequential read Test Address uniquence Test Random address/data Test Cross talk & peek shift Test Write/read/compare(CE) Test Write specified address Test Read specified address Test ECC circuit (CE cylinder) Test
9	Real time	01 02	Real time Test Real time carry set Test
10	NDP	01	NDP Test

ANNEX B : AVERAGE EXECUTION TIME

TEST NO.	TEST NAME	SUBTEST NO.	EXECUTION TIME
1	SYSTEM	01	1 Second
2	MEMORY (640 KB)	01 02 03	59 Seconds 17 Seconds 35 Seconds
3	KEYBOARD	01	
4	DISPLAY	01 02 03 04 05 06 07 08	1 Second 1 Second 1 Second 1 Second 3 Second 7 Second 15 Second 15 Second
5	FDD	01 02 03 04 05	65 Seconds 130 Seconds 12 Seconds 1 Second 1 Second
6	PRINTER	01 02 03	110 Seconds 15 Seconds 1 Second
7	ASYNC/ (RS232C)	01 02 03 04 05 06 07	1 Second 1 Second 1 Second 1 Second 5 Second 10 Second 60 Second

ANNEX B : AVERRAGE EXECUTION TIME (Continued)

TEST NO.	TEST NAME	SUBTEST NO.	EXECUTION TIME
8	HDD	01 02 03 04 05 06 07 08	6 Second 10 Second 30 Second 13 Second 2 Second 1 Second 1 Second 2 Second
9	Real Time	01 02	
10	NDP	01	1 Second

ANNEX C : ERROR STATUS CODE LIST

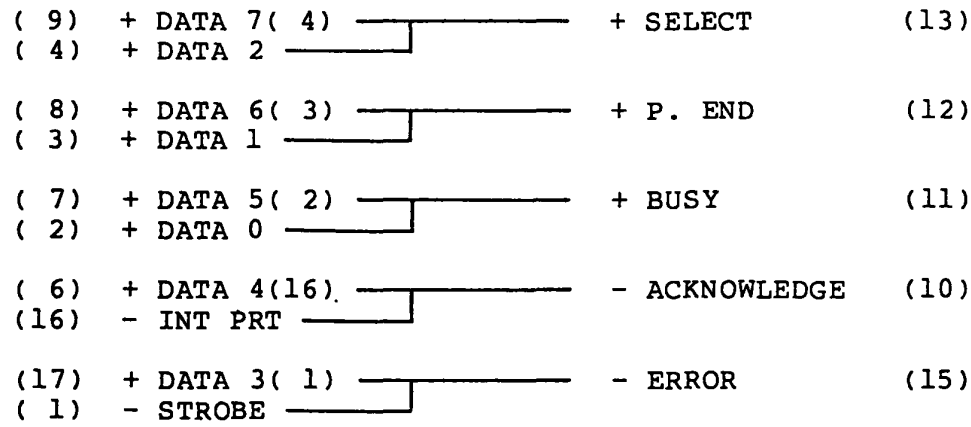
DEVICE NAME	ERROR CODE	STATUS
SYSTEM	01	ROM Checksum Error
MEMORY	01	Parity Error
	02	PROTECTED MODE NOT CHANGE ERROR
COMMON	FF	Compare error
FDD	01	Bad Command
	02	Address Mark Not Found
	03	Write Protected
	04	Record Not Found
	06	Media removed on dual attach card
	08	DMA Overrun Error
	09	DMA Boundary Error
	10	CRC Error
	20	FDC Error
	40	Seek Error
	60	FDD not drive
	80	Time Out Error
PRINTER	01	Time Out
	08	Fault
	10	Select Line
	20	Out of Paper
	40	Power off
	80	Busy Line
ASYNC/ (RS232C)	01	DSR Off Time Out
	02	CTS Off Time Out
	04	RX EMPTY Time Out
	08	TX BUFFER FULL Time Out
	10	Parity Error
	20	Framing Error
	40	Overrun Error
	80	Line Status Error
	88	Modem Status Error
	33	NO CARRIER (CARD MODEM)
	34	ERROR (CARD MODEM)
	36	NO DIAL TONE (CARD MODEM)

ANNEX C ERROR STATUS CODE LIST (Continued)

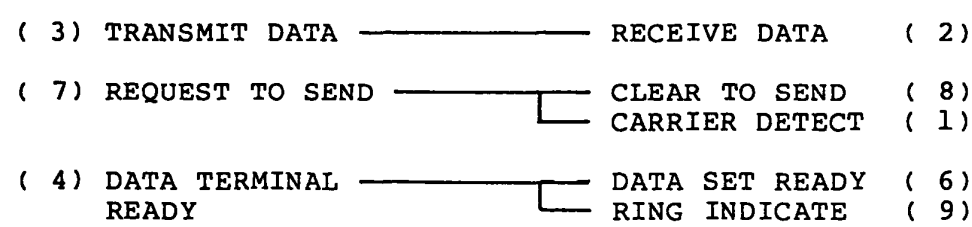
DEVICE NAME	ERROR CORD	STATUS
HDD	01	Bad command error
	02	Bad address mark
	04	Record not found
	05	HDC NOT RESET
	07	Device not initialize
	09	DMA Boundary error
	0A	Bad secter error
	0B	Bad track error
	10	ECC error
	11	ECC recover enable
	20	HDC error
	40	Seek error
	80	Time out error
	AA	Device not ready
	BB	Undefined
	CC	Write fault
	E0	Status error
	F0	Not sense error (HW.code=FF)
NDP	01	NO CO-PROCESSOR
	02	Control word error
	03	Status word error
	04	Bus error
	05	Additional error
	06	Multipul error

ANNEX D : WRAPAROUND CONNECTOR

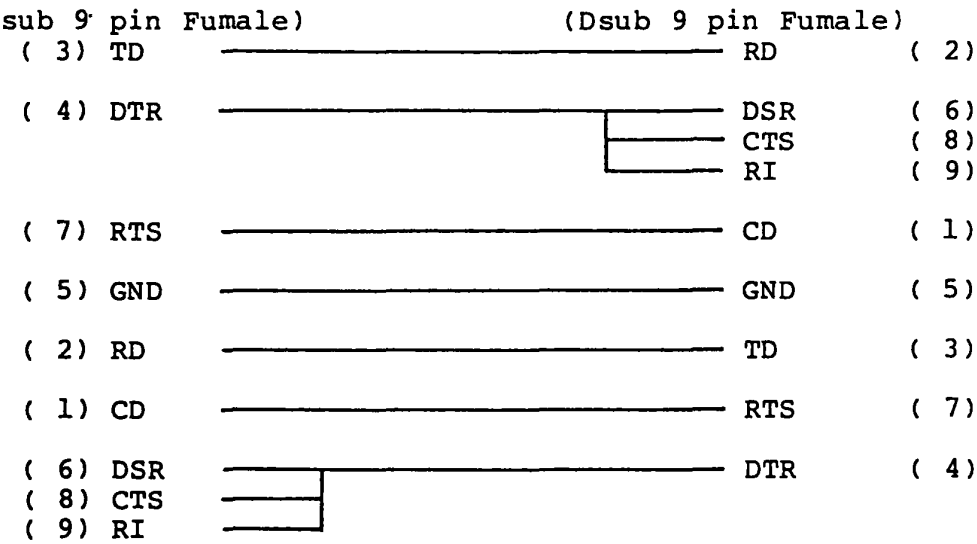
1. Wraparound connector for printer (Dsub 25 pin male)



2. Wraparound connector for RS232C



3. Direct connection cable for RS232C



APPENDIX A

Bus Controller GA (Gate Array)

The Bus Controller Gate Array is a 2,600 gate flat package type with 100 lead chip.
It contains following functions.
Signal name and meaning of each pin, and description of each function block are covered in this section.

1) Clock generator
2) Command decoder
3) Bus controller
4) 8-16 bit conversion controller
5) Wait controller
6) DMA bus controller
7) DMA Page register
8) RAM/ROM select controller
9) NMI controller
10) Keyboard Data Controller
11) Circuitry compatible to 8255
12) TURBO

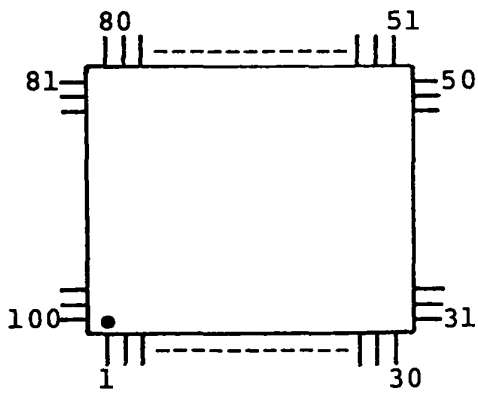
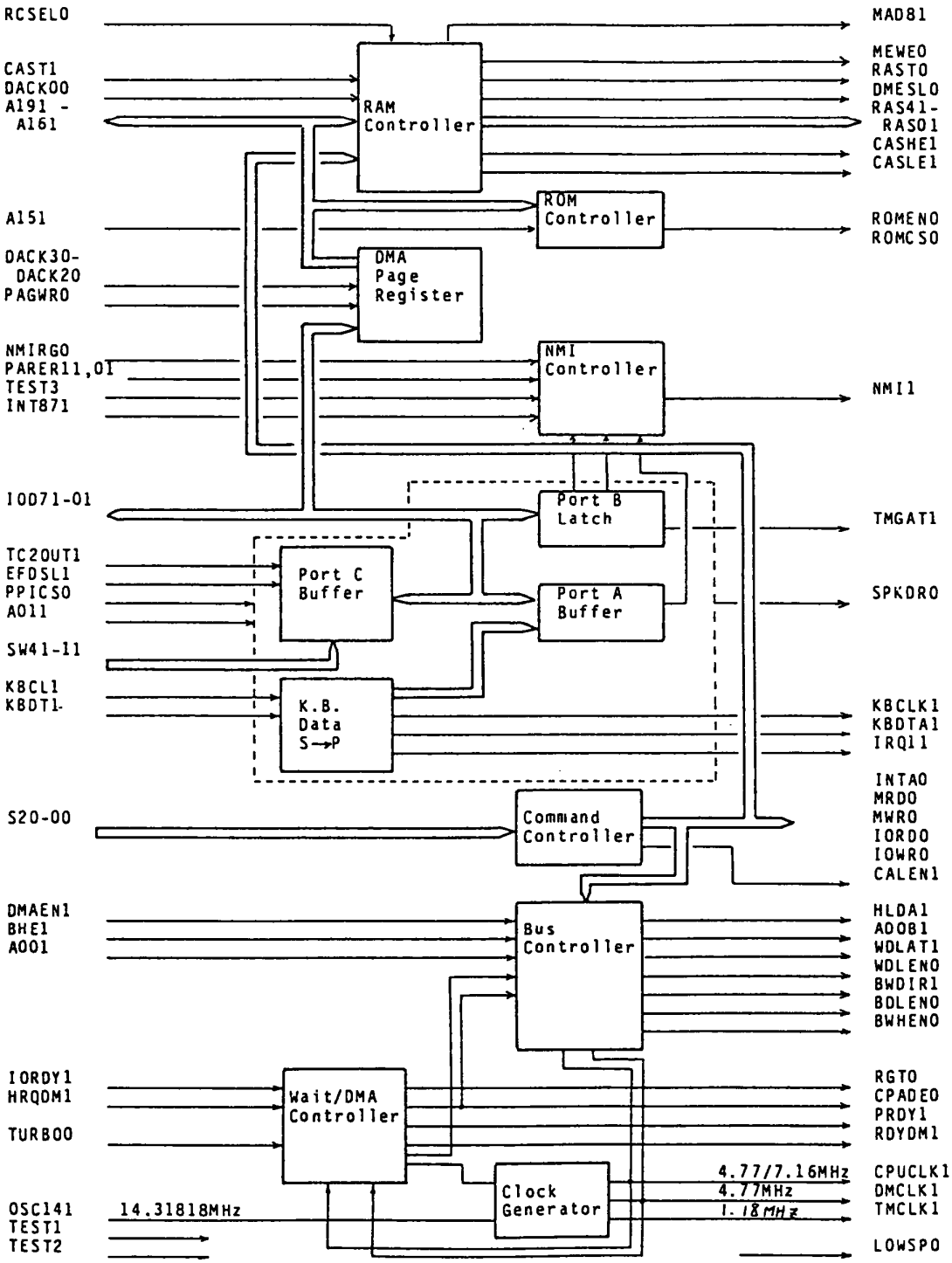


Figure A-1 Bus Controller GA Block Diagram



Interface Signal (In=35, Out=38, I/O=17)

Pin	I/O	Signal Name	Description
1	I	CAST1	CAS timing signal. This signal is generated from delayed RAST.(100 ms)
2	O	KBCLK1	Data transfer clock to Keyboard controller. Low level at Port-B bit6 ="0".
3		Vcc	+5v
4	O	DMCLK1	DMA(82C37) clock, 4.77 MHz.
5	O	KBDTA1	Data to Keyboard controller.
6	I	DACK30	DMA acknowledge signal for channel 3.
7	I	DACK20	DMA acknowledge signal for channel 2.
8	I	DACK00	DMA acknowledge signal for channel 0.
9	I	HRQDM1	DMA request signal from 82C37.
10	I	DMAEN1	DMA address enable signal (A19-A16). This signal is generated from the AEN signal of 82C37.
11	O	RDYDM1	Bus ready signal in a DMA cycle
12	I	KBDT1	Data from the Keyboard controller.
13	I	KBCL1	Clock signal from the Keyboard controller. It is used to transfer data from the Keyboard controller.
14	O	TMCLK1	Clock signal for 82C53.
15		GND	Ground
16	O	TMGAT1	Control signal to gate 2 of 82C53.
17	I	TC2OUT1	Output signal from channnel 2 of 82C53.
18	O	INTA0	Interrupt acknowledge command. Response signal to interrupt request
19	O	IRQ11	Interrupt level 1 signal. (for Keyboard interrupt)
20	I	TEST1	Output command inhibit signal. If "Low", inhibit (command input = mode). If "High", enable (command output = mode).
21	O	ROMEN10	ROM read enable signal. Active Low when (F000 - F7FFF) MERD.
22	O	RAST0	RAS timing signal. This signal is output with RAS0-RAS4 at same time. It is inhibited when memory refresh time.
23	O	RAS11	RAS timing of 128 KB memory block. RAS11 for 128 KB - 256 KB.
24	O	RAS01	RAS01 for 0 - 128 KB.
25	O	CASLE1	CAS timig, low side (even address).
26	O	CASHE1	CAS timig, high side (odd address).
27	O	PRAS1	RAS signal for parity bit. (0 - 512 KB)

Note: Least significant digit of the signal name stands for active level. 0: Low, 1:High

Interface Signal (Continued)

Pin	I/O	Signal Name	Description
28		Vcc	+5v
29	O	RAS21	RAS timing of 128 KB memory block. RAS21 for 256 KB - 384 KB.
30	O	RAS31	RAS31 for 384 KB - 512 KB.
31	O	RAS41	RAS41 for 512 KB - 640 KB.
32	O	MAD81	Address "A8" for 256 K x 1 parity RAM.
33	O	CPADE0	DMA HOLDA signal. CPU address bus is disable/DMA address bus is enable.
34	O	ROMCS0	ROM select signal. (ROM=F0000-FFFFF)
35	O	SPKDR0	Speaker drive signal.
36	I	IORDY1	Bus ready signal.
37	O	AD0B1	Address bit 0.
38	I/O	IOWR0	I/O bus data write command.
39	I/O	IORD0	I/O bus data read command.
40		GND	Ground
41	I/O	MWR0	Memory data write command.
42	I/O	MRD0	Memory data read command.
43	I	PPICS0	PPI select signal. This signal is active low.
44	I	NMIRG0	NMI set signal. This signal is active low.
45	I	PAGWR0	DMA page Reg. write signal.
46	I	TURBO0	Set signal to CPU clock control Reg.
47	O	LOWSP0	CPU clock mode. ("High"=7.16 MHz, "Low"=4.77 MHz)
48	I	PONCL0	Power on clear signal.
49	I	RCSEL0	Timing signal to Row/Column switching.
50	O	ROMEN0	ROM read enable signal. This signal is generated when (F8000-FFFFF)·$\overline{MERD}$.
51	I/O	A191	CPU/DMA address lines. CPU address is input when input mode. DMA page reg. content is output when output mode (DMA cycle). Address line bit 19.
52	I/O	A181	Address line bit 18.
53		Vcc	+5v
54	I/O	A171	Address line bit 17
55	I/O	A161	Address line bit 16
56	I	A151	Address line bit 15.
57	I	A141	Address line bit 14.
58	I	A131	Address line bit 13.
59	O	CALEN1	CPU address latch signal.

Interface Signal (Continued)

Pin	I/O	Signal Name	Description
60	O	HLDA1	Timing signal same to CPADE0 but it goes to Exp. bus.
61	O	WDLAT1	Low data (even) latch signal for word read operation to 8 bit Bus.
62	O	WDLEN0	Low data (even) enable signal for word read operation to 8 bit Bus.
63	O	BDLEN0	Low data (even) enable signal for byte read/write operation.
64	O	BWDIR1	Specifys data direction. Held to be low except IOWR and MEWR to I/O Bus.
65		GND	Ground
66	O	BWHEN0	High data (odd) enable signal for byte or word read/write operation.
67	O	MEWE0	WE timing signal for system RAM.
68	I/O	IOD71	Bidirectional data bus bit 7.
69	I/O	IOD61	Bidirectional data bus bit 6.
70	I/O	IOD51	Bidirectional data bus bit 5.
71	I/O	IOD41	Bidirectional data bus bit 4.
72	I/O	IOD31	Bidirectional data bus bit 3.
73	I/O	IOD21	Bidirectional data bus bit 2.
74	I/O	IOD11	Bidirectional data bus bit 1.
75	I/O	IOD01	Bidirectional data bus bit 0.
76	I	PARER01	Parity bit for odd address data.
77	I	PARER11	Parity bit for even address data.
78		Vcc	+5v
79	I	A001	Address line bit 0.
80	I	A011	Address line bit 1.
81	O	NMI1	Non maskable interrupt signal.
82	O	CPUCLK1	CPU Clock: 4.77 MHz (SLOW) 7.16 MHz (FAST)
83	O	RESET1	Reset pulse. This signal is active high.
84	O	PRDY1	CPU ready signal.
85	I	S00	CPU status signal bit 0.
86	I	S10	CPU status signal bit 1.
87	I	S20	CPU status signal bit 2.
88	I	BHE1	Bus high enable. Decides bus mode, it is used with A0

$\overline{\text{BHE1}}$	A0	Description
0	0	Whole word
0	1	Upper byte - odd address
1	0	Lower byte - even address
1	1	None

Interface Signal (Continued)

Pin	I/O	Signal Name	Description
89	I	INT871	8087 interrupt signal.
90		GND	Ground
91	I/O	RGT0	This gate sends a low pulse to RQ/GT pin of the CPU when the GA receives a HRQDM1 signal from the 82C37. Then it sends a HOLDA1 signal to the 82C37 when it receives a low pulse from the CPU. It also sends a low pulse to the CPU from this gate when the DMA cycle is complete.
92	I	OSC141	Output signal from OSC. 14.31818MHz
93	I	EFDSL1	External FDD select switch signal.
94	O	DMESL0	V-RAM select signal.
95	I	TEST2	If "Low", clock duty is 1/2. If "High", clock duty is 1/3.
96		TEST3	Test pin.
97	I	SW41	Configuration switch signal bit 4.
98	I	SW31	Configuration switch signal bit 3.
99	I	SW21	Configuration switch signal bit 2.
100	I	SW11	Configuration switch signal bit 1.

Followings are summarized descriptions about each functional block in this GA.

1) Clock Generator

The Clock Generator receives 14.31818 MHz clock, then generates CPU clock, DMA clock and Timer clock.

CPU clock : 4.77 MHz/7.16 MHz *
DMA clock : 4.77 MHz (Duty 50%)
Timer clock : 1.18MHz (Duty 50%)

* :CPU clock rate is changed by selecting mode (Fast/Slow). The clock duty is selected to 1/2 or 1/3 by TEST2 pin.

2) Command Decoder

Commands to I/O controller or memory are generated by decoding CPU status.

CPU Status			Command
S2	S1	S0	
0	0	0	INTA0
0	0	1	IORD0
0	1	0	IOWR0
0	1	1	(None)
1	0	0	MERD0
1	0	1	MERD0
1	1	0	MEWR0
1	1	1	(None)

3) Bus Controller

The Bus Controller controrls data bus by decoding commands described paragraph 2).

4) 8 -- 16 bit conversion controller

8 bit -- 16 bit conversion is performed by this circuitry when an 8 bit bus is accessed.
Bus, Wait timing is controlled by this circuitry.

5) Wait Controller

The wait controller decides CPU wait cycle according to the each command described paragraph 2) by Bus Ready signal.
The basic cycle timing of the each command is as follows.

Command	CPU Clock Rate	
	7.16 MHz	4.77 MHz
RAM(System RAM)	4T	4T(6T)
ROM(Byte)	5T	4T(6T)
ROM(Word)	10T	8T(12T)
I/O Bus(Byte)	6T	5T(7.5T)
I/O Bus(Word)	12T	10T(15T)
DMA	5T	5T(7.5T)

Note: The cycle timing with parenthesises is counted as the cycle timing under the clock rate of 7.16 MHz.

6) DMA Bus Controller

The DMA Bus Controller issues DMA request signal and controls bus. It issues a bus disconnection request signal (RQ/GT) to the CPU as a response to the DMA request from the DMAC. It issues HOLDA1 signal to DMAC when the bus is disconnected, then DMA cycle starts. After the DMA cycle is complete, it changes the bus connection to the CPU by sending a signal to the RQ/GT gate of the CPU.
The Output of I/O address decoder is inhibited during a DMA cycle.

7) DMA Page Register

This register is to save the most significant 4 bits of the address lines (A19 - A16) during a DMA cycle.
It is composed of 3 sets of 4-bit registers and they are assigned to the following I/O addresses.

I/O Address	Command	Description
081	IOWR	DMA Channel 2 Page Register 7 ----- 4 | 3 | 2 | 1 | 0 | | A19 | A18 | A17 | A16 |
082	IOWR	DMA Channel 3 Page Register
083	IOWR	DMA Channel 0 and 1 Page Register

8) RAM/ROM Select Controller

This circuit is for RAM/ROM address select control on the system board.
It issues $\overline{RAS}/\overline{CAS}$ signals to the RAM and ROM for the control.

A). RAM select on the system board.
It uses the informations of address signal (0 - 640 KB) and configuration DIP switches on the system board for the RAM selection.

384

DIP Switch		Memory Size
SW3	SW2	
0	0	256 KB (00000 - 3FFFF)
0	1	384 KB (40000 - 5FFFF) ←
1	0	512 KB (60000 - 7FFFF)
1	1	640 KB (80000 - 9FFFF)

"0" = ON
"1" = OFF

B). RAM/ROM Selection.
RAM/ROM select signals are generated from address signals as follows.

Address							Memory Select Signal
19	18	17	16	15	14	13	
0	0	0	-	-	-	-	RAS0 (00000 - 1FFFF)
0	0	1	-	-	-	-	RAS1 (20000 - 3FFFF)
0	1	0	-	-	-	-	RAS2 (40000 - 5FFFF)
0	1	1	-	-	-	-	RAS3 (60000 - 7FFFF)
1	0	0	-	-	-	-	RAS4 (80000 - 9FFFF)
0	-	-	-	-	-	-	PRAS (00000 - 7FFFF)
1	1	1	1	0	-	-	ROMEN10(F0000 - F7FFF)
1	1	1	1	1	-	-	ROMEN0 (F8000 - FFFFF)
1	0	1	1	-	-	-	DMSL (B0000 - BFFFF)
1	1	0	0	-	-	-	DMSL (C0000 - CFFFF)

C). Refresh Address Control.
The refresh address of the RAM is given by DMA address (A7 - A0). But RAM address is given as A1 - A16.
A16 is input as a least significant bit (A0) of ROW address of the RAM, and it is changed to as A0.
A0 is used for ODD/EVEN selection of the data bus except refresh cycle.
Note: "AD8" of the 256 KB RAM (for parity-bits) is given by switching A17 and A18. ROW(A17)/COLUMN(A18) selection is done by "RCS0" signal.

)) NMI Controller.

This circuitry is to send a NMI (Non Maskable Interrupt) signal to the CPU when it detects a memory parity error or 8087 Interrupt.
Parity detection is controlled by PB4 bit of the PPI. If the PB4 is "0", it can detect an error but if the PB4 is "1", it can not detect an error.
The output of the NMI is controlled by NMI register. If "1" is set to NMI register, the output is enable but if "0" is set, the output is disable.
The NMI register is reset to "0" when power is turned on, and it is set by writing "80h" to I/O address "0Axh" (x:don't care).
It is also reset to "0" when "0" is written to I/O address "0Axh".

Clear Mask : * When Power On Reset.
* When "00h" is written to I/O address "0Axh".

Set Mask : * When "80h" is written to I/O address "0Axh".

Note: When the system is 256 KB memory type, parity check is not performed. If the system has expansion memory unit, parity check is performed.
The parity generator is contained within the Bus Controller GA, and the parity bit RAM is contained within the expansion memory board.
Error detecting function is inhibited when the RAM switch is set to 256 KB memory size.

10) Keyboard (K.B.) Data Controller.

This circuitry is to receive bit-serial data from the K.B. controller (80C49), then the data is converted to parallel data. If the PB7 is "0", the converted parallel data is enabled to be output to the PA but if the PB7 is "1", the output is disabled and K.B. data is cleared. When the PB6 is "0", K.B. clock is inhibited but if the PB6 is "1", it becomes to be enabled. The K.B. data is composed of 8 bit data with a leading start bit total of 9 bits. When the circuitry receives one byte data from the K.B. controller, then it inhibits to receive any more data and issues interrupt signal (IRQ1).
The latch timing of each data bit from the K.B. controller is at a time of when K.B. clock is low and rising point of second DMA CLK pulse.

11) Circuitry Compatible to 8255.

This circuitry is compatible to intel 8255 (PPI) chip.
It contains Port-A, B, C and mode control register.

A). Port A (I/O address = "060h").
Data setting to the register is performed by writing to the I/O address "060h".
Getting the data from the register is performed by reading the same address after setting "0" to bit 4 of the mode register. Bit 4 of the mode register is usually set to "1" (when power on reset.) and the following data is gotten when read operation is executed.

when Mode Reg. bit 4 ="1"

	Bit	PB7="0"	PB7="1"
	PA 0	Input Keyboard Data	
I	1		
N	2		
P	3		
U	4		
T	5		
	6		
	7		

B). Port B (I/O address = "061h").
Data setting to the register is performed by writing to the I/O address "061h".
Getting the data from the register is performed by reading the same address. The meaning of each bit of the register is as follows.

	Bit	Description
	PB 0	+ Timer 2 gate speaker
O	1	+ Speaker data
U	2	Not used
T	3	Read High/Low switch
P	4	- Enable RAM parity check
U	5	- Enable I/O channel check
T	6	- Hold keyboard CLK low
	7	- (Enable keyboard), + (CLR K.B.)

Each bit of the register (PC bit) after power on reset is as follows.

Bit	7	6	5	4	3	2	1	0
State	1	0	1	1	1	1	0	0

C). Port C (I/O address = "062h")
Data setting to the register is performed by writing to the I/O address "062h".
Getting the data from the register is performed by reading the same address when bit 0 (PC0-3) and bit 3 (PC4-7) of the mode control register are set to "0".
Bit 0 and 3 of the mode register are usually set to "1" (when power on reset.) and the following data is gotten when read operation is executed.

when Mode Reg. bit 0,3 ="1"

	Bit	PB3="0"	PB3="1"
I	PC 0	"1" (Fixed)	"0" (Fixed)
N	1	87 install (*SW1)	"1" (Fixed)
P	2	RAM size 0 (*SW2)	Drive 0 (*SW4)
U	3	RAM size 1 (*SW3)	"0" (Fixed)
T	4	+ Speaker drive signal	
	5	+ Timing channel 2 out	
	6	+ I/O channel check	
	7	+ RAM parity check	

*SW1

SW1	8087 Install
0	87 is not installed
1	87 is installed

0 = ON
1 = OFF

*SW3,SW2

SW3	SW2	Memory Size
0	0	256 KB
0	1	384 KB
1	0	512 KB
1	1	640 KB

*SW4

SW4	Number of FDD
0	1
1	2

D). Mode Control Register (I/O address = "063h").
This register is set as follows by writing the data "99h" or "FFh" to the address "063h" or power on reset.

Bit	7	6	5	4	3	2	1	0
State	1	x	x	1	1	x	x	1

x: don't care

Bit	State	Description
0	0	PC latch data (PC0-3) is selected as read data of PC0-3.
	1	SW data is selected as read data of PC0-3.
3	0	PC latch data (PC4-7) is selected as read data of PC4-7.
	1	Status information is selected as read data of PC4-7.
4	0	PA latch data is selected as read data of PA.
	1	K.B. data is selected as read data of PA.
7	0	----------
	1	Enables to set mode control register. Resets PortA, PortB, PortC.

APPENDIX B

I/O Controller GA (Gate Array)

The I/O Controller Gate Array is a 1,500 gate flat package type with 100 lead chip.
Two I/O Controller Gate Arrays are used on the system PCB.
It pritends as I/O Decoder Gate Array or Bus Driver Gate Array by selecting the voltage level of 50 pin of the GA.

1) I/O Decoder GA

The I/O Decoder GA is to decode I/O chip selection.
It is composed of Printer port, precompensation circuit for FDD write data and DMA request signal delay circuit.

2) Bus Driver GA

The Bus Driver GA is composed of data busses and address busses between the CPU and memory,I/O devices.

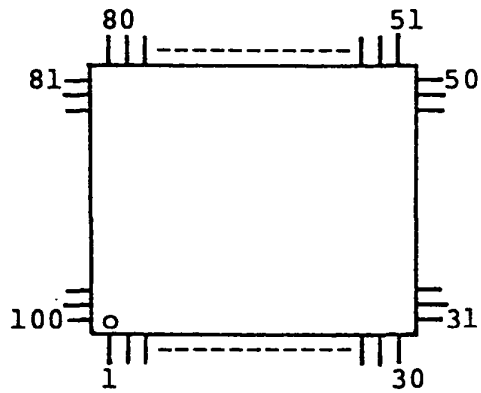
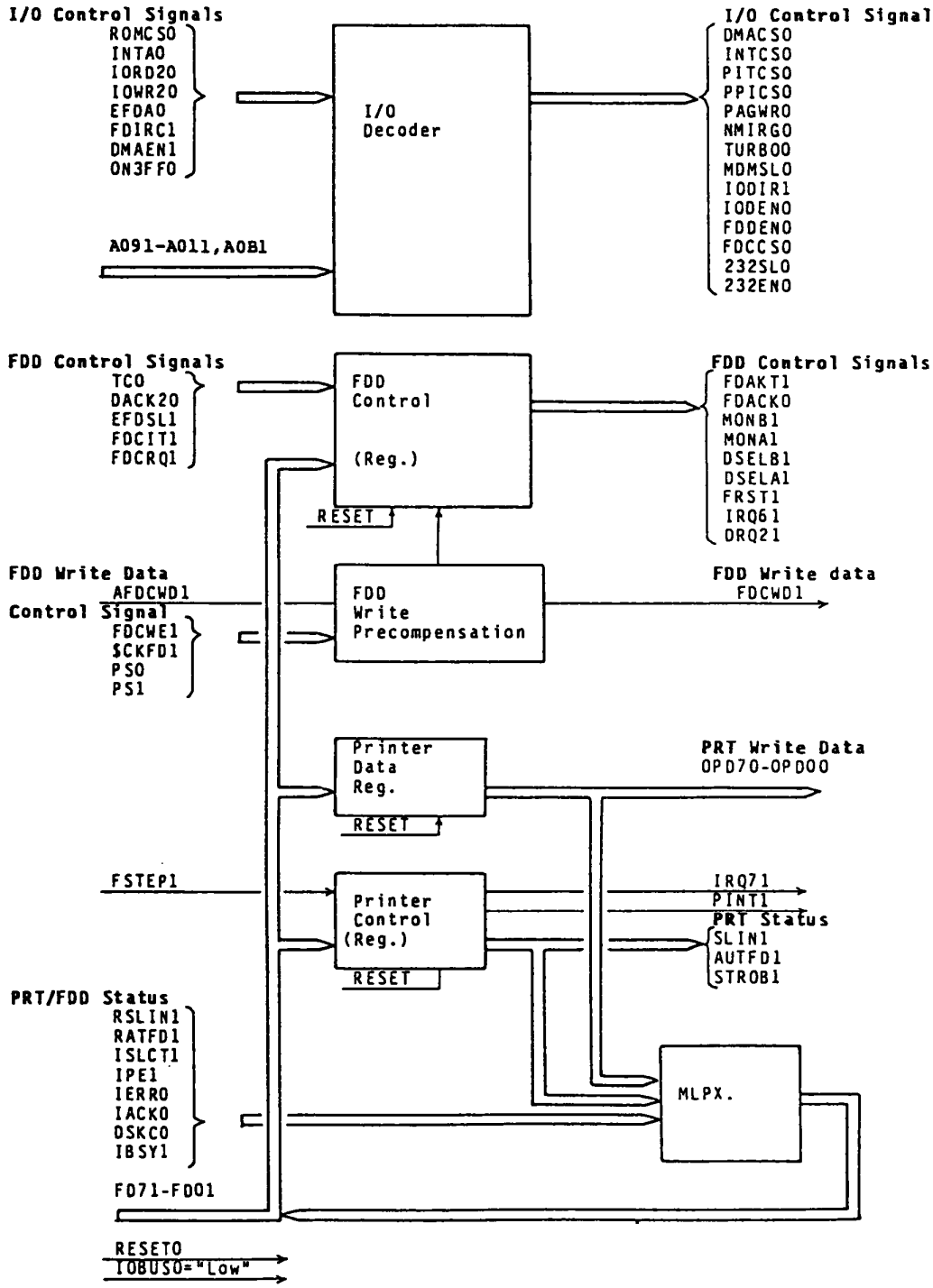


Figure B-1 I/O Decoder GA Block Diagram



I/O Decoder GA Interface Signal

Pin	I/O	Signal Name	Description
1	I	ROMCS0	ROM select signal.
2	O	PPICS0	8255 (compatible circuit) register select signal. This signal is active when address is 060h-07Fh.
3		VCC	+5v
4		GND	Ground
5	O	PAGWR0	DMA page register set signal. This signal is active when (080h-09Fh). IOW is made.
6	O	TURBO0	TURBO register (FAST/SLOW) set signal. This signal is active when address is 0E0h-0FFh.
7	I	TC0	Terminal count signal from 8237.
8	I	DACK20	ACK signal of channel 2 of DMA.
9	I	INTA0	Interrupt acknowledge signal from the Bus Controller GA.
10	O	DMACS0	DMAC (82C37) select signal. This signal is active when address is 0-01Fh.
11	O	PITCS0	82C53 select signal. This signal is active when address is 040h-05Fh.
12	O	INTCS0	82C59 select signal. This signal is active when address is 020h-03Fh.
13	O	232EN0	Bus enable signal to the Real Timer and RS232C.This signal is active when Real Timer or RS232C is selected.
14	O	FDDEN0	Printer/FDD data bus enable signal.
15		GND	Ground
16	O	IRQ71	Printer interrupt signal. This signal is sent to IRQ7 pin of the 8259.
17	O	IRQ61	FDD interrupt signal . This signal is sent to IRQ6 pin of the 8259.
18	O	DRQ21	DMA request signal. This signal is sent to 8237 (DMAC).
19	I	ON3FF0	This signal changes the address of RS232C register and MODEM register.
20	I	DSKC0	Disk change signal from the FDD.
21	I	A091	A091-A011,A0B1 are address lines which are used to decode a I/O address. Address line bit 9.
22	I	A081	Address line bit 8.
23	I	A071	Address line bit 7.
24	I	A061	Address line bit 6.
25	I	A051	Address line bit 5.
26	I	A041	Address line bit 4.
27	I	A031	Address line bit 3.

I/O Decoder GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
28		NO USE	(Open)
29		NO USE	(Open)
30	I	A011	Address line bit 1.
31	O	MDMSL0	MODEM register select signal. When ON3FF0="High", ...3F8h-3FFh. When ON3FF0="Low", ...2F8h-2FFh.
32	O	232SL0	RS232C register select signal. When ON3FF0="High".... 2F8h-2FFh. When ON3FF0="Low" .... 3F8h-3FFh.
33	I	PRTIN0	Ground
34	I	EFDA0	FDD drive number assignment signal. External FDD is assigned to the drive #1, when this signal is "Low".
35	I	A021	Address line bit 2.
36	I	RESET0	Reset signal. This signal is active low.
37	I	EFDSL1	Printer/External FDD switching signal. If this signal is "high", the PRT/FDD connector is reserved for FDD interface.
38	I	$CKFD1	Same clock signal to the clock signal sent from the VFO to the FDC.
39	O	FDCCS0	FDC chip select signal.
40		GND	Ground
41	I	FDCIT1	FDC interrupt signal. This signal comes from INT pin of the FDC.
42	O	NMIRG0	NMI register set signal. This signal is active when (0A0h-0BFh).IOW is made.
43	O	FDAKT1	This signal goes to terminal pin of the FDC. (termination of R/W operation)
44	O	FDACK0	Response signal to DMA request signal from the FDC. This signal is sent to the FDC.
45	I	FDCRQ1	DMA cycle request signal from the FDC.
46	O	FRST1	FDC reset signal.
47	I	FDIRC1	FDD seek direction signal from the FDC.
48	I	IBSY1	Busy status from the Printer.
49	I/O	FD71	Local data bus for the Printer/FDD bit 7.
50	I	IOBUS0	Function select signal of the GA. When this signal is high, the GA acts as I/O decoder.
51	I	RATFD1	Wraparound signal from the Printer control register.
52	I	RSLIN1	Wraparound signal from the Printer control register.

I/O Decoder GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
53		VCC	+5v
54		GND	Ground
55	I	IERR0	Error status from the printer.
56	I	IACK0	ACK signal from the Printer.
57	I	ISLCT1	Status signal from the Printer.
58	I	IPE1	Status signal from the Printer.
59	O	AUTFD1	Printer control signal from the Printer control register.
60	O	STROB1	Printer control signal from the Printer control register.
61	O	SLIN1	Printer control signal from the Printer control register.
62	O	OPD00	Printer data bit 0.(from PRT data reg.)
63	O	OPD10	Printer data bit 1.(from PRT data reg.)
64	O	OPD20	Printer data bit 2.(from PRT data reg.)
65		GND	Ground
66	O	OPD30	Printer data bit 3.(from PRT data reg.)
67	O	OPD40	Printer data bit 4.(from PRT data reg.)
68	O	OPD50	Printer data bit 5.(from PRT data reg.)
69	O	OPD60	Printer data bit 6.(from PRT data reg.)
70	O	OPD70	Printer data bit 7.(from PRT data reg.)
71	I/O	FD01	Local data bus for the PRT/FDD bit 0.
72	I/O	FD11	Local data bus for the PRT/FDD bit 1.
73	I/O	FD21	Local data bus for the PRT/FDD bit 2.
74	I/O	FD31	Local data bus for the PRT/FDD bit 3.
75	I/O	FD41	Local data bus for the PRT/FDD bit 4.
76	I/O	FD51	Local data bus for the PRT/FDD bit 5.
77	I/O	FD61	Local data bus for the PRT/FDD bit 6.
78		VCC	+5v
79		GND	Ground
80	O	PINT1	Printer control signal from the Printer control register.
81	O	DSELA1	Drive #1 select signal to the FDD.
82	O	MONA1	Moter on signal to the FDD drive #1.
83	O	DSELB1	Drive #2 select signal to the FDD.
84	O	MONB1	Motor on signal to the FDD drive #2.
85	I	FSTEP1	Step pulse to the FDD.
86	I	DMAEN1	DMA cycle indicating signal.
87	I	IORD20	I/O read command.
88	I	A0B1	Address line bit 0.
89	I	IOWR20	I/O write command.
90		GND	Ground

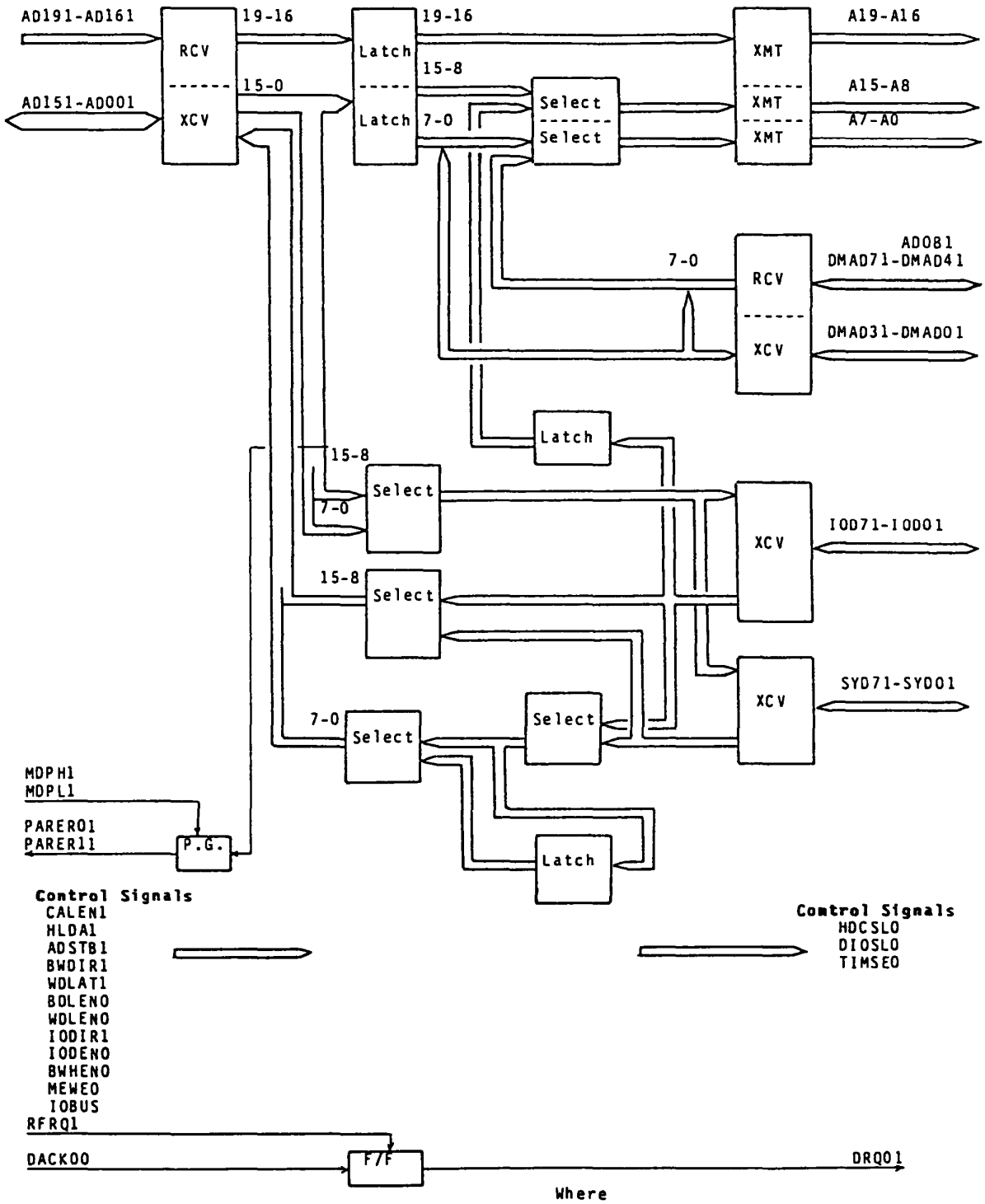
I/O Decoder GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
91	I	CHENG	FDD write precompensation control signal. This signal is fixed to low for the T1100 PLUS system.
92	I	NO USE	Ground
93	I	NO USE	Ground
94	O	FDCWD1	FDD write data.
95	I	PS1	FDD write precompesation control signal. This signal is fixed to low for the T1100 PLUS system.
96	I	PS0	FDD write precompesation control signal. This signal is fixed to low for the T1100 PLUS system.
97	I	AFDCWD1	FDD write data from the FDC.
98	O	FDCWE1	FDD write enable signal from the FDC.
99	O	IODEN0	I/O data bus enable signal to the Bus Driver GA.
100	O	IODIR1	I/O data bus direction signal to the Bus Driver GA. This signal is low when I/O read operation.

Bus Driver GA (Gate Array)

The function of Bus Driver GA is implemented in the I/O Control GA. When the IOBUS (50 pin) is set to Ground, the I/O Control GA acts as the Bus Driver GA and following signal names and their functions are applied to the GA.

Figure B-2 Bus Driver GA Block Diagram



Bus Driver GA Interface Signal

Pin	I/O	Signal Name	Description
1	O	A011	A151-A001 are least significant 16-bits of adddress lines from this GA. Address line bit 1.
2	O	A001	Address line bit 0.
3		VCC	+5v
4		GND	Ground
5	O	PARER01	Parity error of address lines AD151-AD081. It is active high.
6	I/O	IOD01	IOD71-IOD01 are bidirectional 8-bit data bus. Data is output when IODIR1.$\overline{\text{IODEN0}}$. Bidirectional data bus line bit 0.
7	I/O	IOD11	Bidirectional data bus line bit 1.
8	I/O	IOD21	Bidirectional data bus line bit 2.
9	I/O	IOD31	Bidirectional data bus line bit 3.
10	I/O	IOD41	Bidirectional data bus line bit 4.
11	I/O	IOD51	Bidirectional data bus line bit 5.
12	I/O	IOD61	Bidirectional data bus line bit 6.
13	I/O	IOD71	Bidirectional data bus line bit 7.
14	I	MEWE0	WE timing signal for the system RAM.
15		GND	Ground.
16	I	BWHEN0	Bus enable signal. This signal is used with $\overline{\text{BWDIR1}}$ signal. When $\overline{\text{BWHEN0}}$.BWDIR1, AD151-$\overline{\text{AD081}}$ → $\overline{\text{SYD}}$71-SYD01(or IOD71-IOD01). When $\overline{\text{BWHEN0}}$.$\overline{\text{BWDIR1}}$, AD151-AD081 ← SYD71-SYD01(or IOD71-IOD01).
17	I	BWDIR1	Bus direction signal. This signal becomes low while CPU/DMA-I/O read cycle.
18	I	BDLEN0	Bus enable signal. This signal is used with $\overline{\text{BWDIR1}}$. When $\overline{\text{BDLEN0}}$.BWDIR1 is made, AD071-$\overline{\text{AD001}}$ → $\overline{\text{SYD}}$71-SYD01(or IOD71-IOD01). When $\overline{\text{BDLEN0}}$.$\overline{\text{BWDIR1}}$ is made, AD071-AD001 ← SYD71-SYD01(or IOD71-IOD01).
19	I	WDLEN0	This signal is enable signal to send data which is latched by WDLAT1 signal to the AD071-AD001.
20	I	WDLAT1	Latch signal for the data from SYD71-SYD01 or IOD71-IOD01.
21	I	HLDA1	This signal is low when it is CPU mode, and high when it is DMA mode. When Low: AD191-AD001 → A191-A001. When high: IOD71-IOD01 → A151-A081 DMAD71-DMAD01 → A071-A001.

Bus Driver GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
22	I	CALEN1	Data on the AD191-AD001 is latched at the trailing edge of the CALEN1.
23	O	A131	Address line bit 13.
24	O	A141	Address line bit 14.
25	O	A151	Address line bit 15.
26	O	A161	A191-A161 are most significant 4-bits of adddress lines from this GA. Address line bit 16.
27	O	A171	Address line bit 17.
28		Vcc	+5v
29		GND	Ground
30	O	A191	Address line bit 19.
31	I	RFRQ1	Memory refresh signal. This signal makes DRQ01 signal to be high at the leading edge of RFRQ1 signal.
32	O	A021	Address line bit 2.
33	O	A031	Address line bit 3.
34	O	A041	Address line bit 4.
35	O	A051	Address line bit 5.
36	O	A061	Address line bit 6.
37	O	A071	Address line bit 7.
38	O	A081	Address line bit 8.
39	O	A091	Address line bit 9.
40		GND	Ground
41	O	A101	Address line bit 10.
42	O	A111	Address line bit 11.
43	O	A121	Address line bit 12.
44	I	DACK00	When memory refresh cycle, this signal becomes to be low and it makes the DRQ01 to be inactive.
45	I	ADSTB1	Latch signal for the data on IOD71-IOD01. The data is latched at the trailing edge of ADSTB1 signal.
46	O	DRQ01	DMA request (Refresh request) signal.
47	I/O	MDPL1	Parity bit for AD071-AD001.
48	I/O	MDPH1	Parity bit for AD151-AD081.
49	I	AD0B1	System address bit 0.
50	I	IOBUS	Function select signal of the GA. When this signal is high, the GA acts as I/O decoder. When this signal is low, the GA acts as Bus driver.
51	O	A181	Address line bit 18.

Bus Driver GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
52	I/O	DMAD01	DMAD31-DMAD01 are bidirectional bus. Data direction on the bus is depend on level of HLDA1. When HLDA1=low: AD031-AD001 are output to the bus. When HLDA1=high: Data on the bus is input to the GA, then output to A031-A001.
53		VCC	+5v
54		GND	Ground
55		GND	Ground
56	O	PARER11	Parity error line of AD071-AD001. When this signal is high, parity error.
57	I	IODEN0	I/O data bus (IOD71-IOD01) enable signal. This signal is used with IODIR1 signal. When IODEN0.IODIR1 is made, IOD71-IOD01 are used as output lines. When IODEN0.IODIR1 is made, IOD71-IOD01 are used as input lines.
58	I	IODIR1	I/O data bus (IOD71-IOD01) direction signal. This signal is used with IODEN0 signal.
59	O	HDCSL0	HDC select signal. This signal is issued when the I/O address is 1F0h-1FFh.
60	O	TIMSE0	Timer IC (TC8250) select signal. This signal is issued when the I/O address is 2C0h-2DFh.
61	O	DIOSL0	Display controller select signal. This signal is issued when the I/O address is 3D0h-3DFh.
62	I/O	SYD01	SYD71-SYD01 are bidirectional 8-bit data bus. When BWDIR1.(BDLEN0+BWHEN0) is made, they act as output lines. Bidirectional data bus bit 0.
63	I/O	SYD11	Bidirectional data bus bit 1.
64	I/O	SYD21	Bidirectional data bus bit 2.
65		GND	Ground
66	I/O	SYD31	Bidirectional data bus bit 3.
67	I/O	SYD41	Bidirectional data bus bit 4.
68	I/O	SYD51	Bidirectional data bus bit 5.
69	I/O	SYD61	Bidirectional data bus bit 6.
70	I/O	SYD71	Bidirectional data bus bit 7.
71	I	DMAD71	DMAD71-DMAD01 are address lines in DMA mode. DMA address line bit 7.

Bus Driver GA Interface Signal (continued)

Pin	I/O	Signal Name	Description
72	I	DMAD6l	DMA address line bit 6.
73	I	DMAD5l	DMA address line bit 5.
74	I	DMAD4l	DMA address line bit 4.
75	I/O	DMAD3l	DMAD3l-DMAD0l are bidirectional bus. When HLDAl=low, they act as output lines. The output data are AD03l-AD00l. When HLDAl=high,they act as input lines. Bidirectional bus bit 3.
76	I/O	DMAD2l	Bidirectional bus bit 2.
77	I/O	DMAD1l	Bidirectional bus bit 1.
78		VCC	+5v
79		GND	Ground
80	I/O	AD00l	AD15l-AD00l are bidirectional address data lines between the CPU and this GA. Address data line bit 0.
81	I/O	AD01l	Address data line bit 1.
82	I/O	AD02l	Address data line bit 2.
83	I/O	AD03l	Address data line bit 3.
84	I/O	AD04l	Address data line bit 4.
85	I/O	AD05l	Address data line bit 5.
86	I/O	AD06l	Address data line bit 6.
87	I/O	AD07l	Address data line bit 7.
88	I/O	AD08l	Address data line bit 8.
89	I/O	AD09l	Address data line bit 9.
90		GND	Ground
91	I/O	AD10l	Address data line bit 10.
92	I/O	AD11l	Address data line bit 11.
93	I/O	AD12l	Address data line bit 12.
94	I/O	AD13l	Address data line bit 13.
95	I/O	AD14l	Address data line bit 14.
96	I/O	AD15l	Address data line bit 15.
97	I	AD16l	AD19-AD16 are address lines from the CPU. Address line bit 16.
98	I	AD17l	Address line bit 17.
99	I	AD18l	Address line bit 18.
100	I	AD19l	Address line bit 19.

APPENDIX C

Display Controller GA (Gate Array)

The Display Controller Gate Array is a 5,000 gates, CMOS, 100-pin flat package type chip.
It contains Color Graphics Adaptor which is able to control external CRT disply as well as internal plasma display.
The Display Controller Subsystem can control following three types of displays.
The signal name and it's meaning of each pin are described in this section.

A). 640 x 400 dot Plasma Display.

B). 640 x 200 dot LCD (Liquid Crystal Display).

C). 640 x 200 dot CRT (Cathode Ray Tube) Display.

Note: External CRT display unit and internal plasma/LCD display unit could not display a screen at same time.
You can select current display unit from them by keyboard operation.

Ctrl + Alt + Home —— Internal display unit is selected.

Ctrl + Alt + End —— External display unit is selected.

The Display Controller GA is composed of following functions.

1) Plasma/LCD/CRT control function.
   This function is compatible with the MC6845 (CRTC) on software operation.

2) Attribute handling function.

3) Interface to CPU (I/O bus).

4) Interface to V-RAM, CG-ROM (Character Generator ROM).

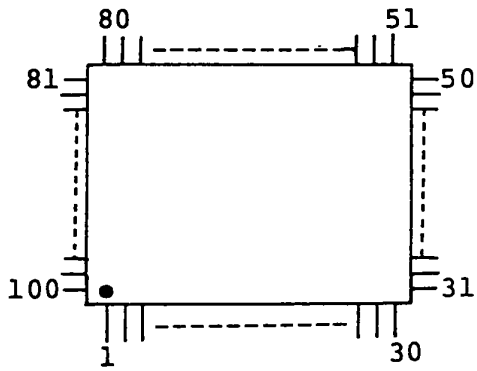
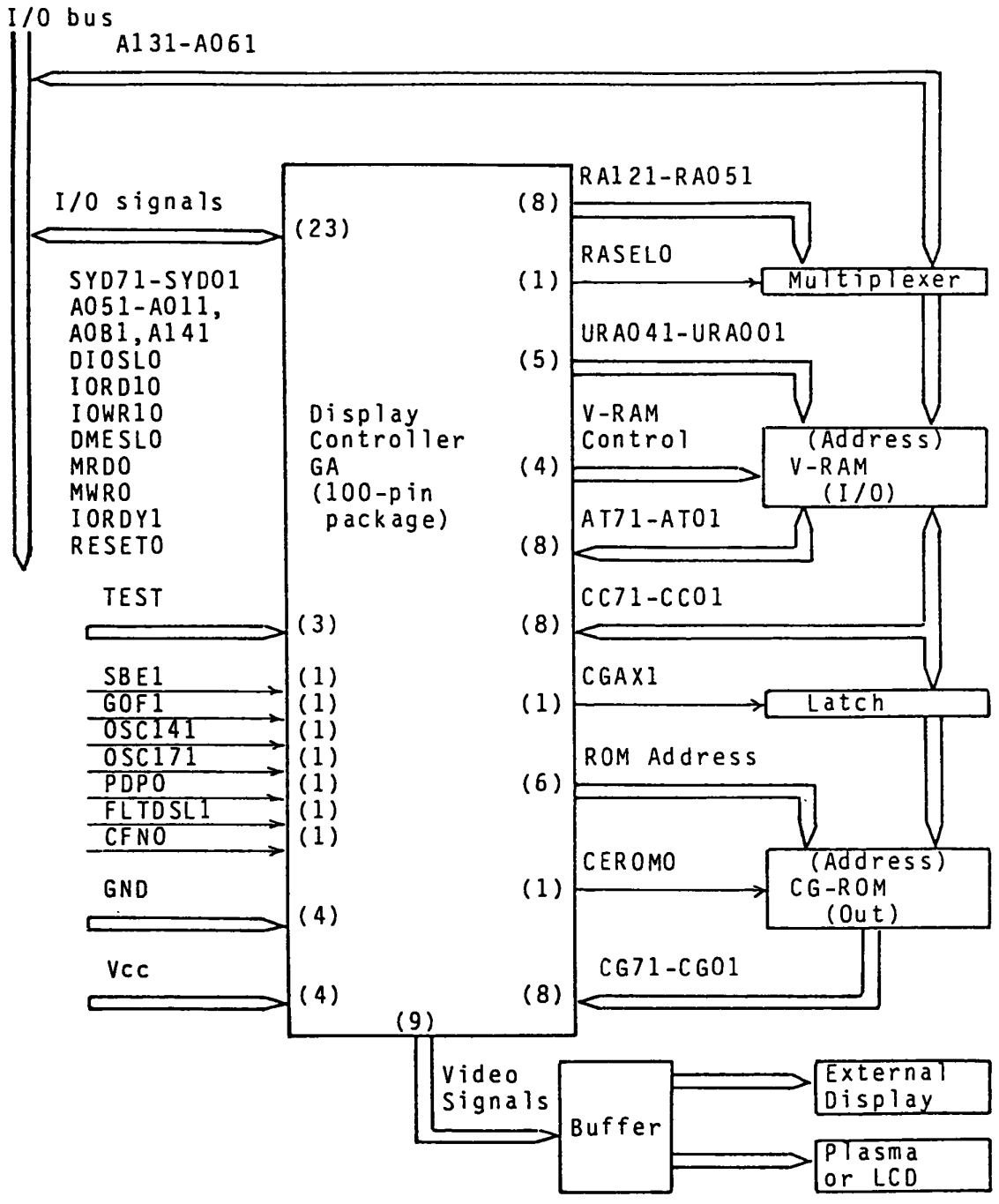


Figure C-1 Display Controller Subsystem (DCS)



Interface Signal

Pin	I/O	Signal Name	Description
1	I	CG31	Character generator output signal bit 3.
2	I	CG41	Character generator output signal bit 4.
3	I	VCC	+5V
4	I	CG51	Character generator output signal bit 5.
5	I	CG61	Character generator output signal bit 6.
6	I	CG71	Character generator output signal bit 7.
7	I	CEROM0	Chip enable signal for CG-ROM (Character Generator - ROM).
8	I	CG21	Character generator output signal bit 2.
9	I	CG11	Character generator output signal bit 1.
10	I	CG01	Character generator output signal bit 0.
11	O	RSA01	Raster scan address bit 0.
12	O	RSA11	Raster scan address bit 1.
13	O	RSA21	Raster scan address bit 2.
14	O	RSA31	Raster scan address bit 3.
15		GND	Ground
16	I	SBE1	Reserved for LCD.(Ground)
17	O	INTEN1	Intensified font select signal. (single dot/double dots character)
18	O	CGM01	Plasma font selection. (8x8/8x16)
19	O	CGAX1	CG address latch.
20	O	RASEL0	Refresh address selection
21	O	RA121	Refresh address bit 12.
22	O	RA111	Refresh address bit 11.
23	O	RA101	Refresh address bit 10.
24	O	RA091	Refresh address bit 09.
25	O	RA081	Refresh address bit 08.
26	O	RA071	Refresh address bit 07.
27	O	RA061	Refresh address bit 06.
28	I	VCC	+5V
29	O	RA051	Refresh address bit 05.
30	I	OSC141	Clock 14.31818 MHz for the video signal of CRT display.
31	I	DIOSL0	Display I/O selected. Access signal to the I/O port of the GA.
32	I	DMESL0	V-RAM access signal for CPU or DMAC.
33	I/O	SYD71	Data bus bit 7.
34	I/O	SYD61	Data bus bit 6.
35	I/O	SYD51	Data bus bit 5.
36	I/O	SYD41	Data bus bit 4.
37	I/O	SYD31	Data bus bit 3.
38	I/O	SYD21	Data bus bit 2.
39	I/O	SYD11	Data bus bit 1.

Interface Signal (Continued)

Pin	I/O	Signal Name	Description
40		GND	Ground.
41	I/O	SYD01	Data bus signal bit 0.
42	O	IORDY1	I/O ready signal.
43	I	RESET0	GA reset signal.
44	I	A051	CPU address bit 5.
45	I	A041	CPU address bit 4.
46	I	A031	CPU address bit 3.
47	I	A021	CPU address bit 2.
48	I	A011	CPU address bit 1.
49	I	A141	CPU address bit 14.
50	I	MWR0	Memory write signal. (for V-RAM write)
51	I	MRD0	Memory read signal. (for V-RAM read)
52	I	IORD10	I/O read signal. It read out I/O port data to the data bus BD00-BD07.
53	I	VCC	+5v
54	I	IOWR10	I/O write signal. It write data on the data bus to the I/O port.
55	I	A0B1	CPU address bit 0.
56	I	PDP0	Plasma display panel select.
57	I	GOF1	GA off. If this signal is high, the GA becomes to be disable.
58		TEH1	Ground
59		TFU1	Ground
60		TCN1	Ground
61	O	BFR0	Video signal.
62	O	FRHV1	Video signal. ~~Vertical~~ sync. signal for composite CRT display.
63	O	FPVS1	Video signal. Vertical sync. signal for plasma/RGB CRT display.
64	O	SXVD1	Video signal.
65	O	GND	Ground.
66	O	LPHS1	Video signal. Horizontal sync. signal for plasma/RGB CRT display.
67	O	D1R1	Video signal. Red signal for RGB CRT display.
68	O	D2G1	Video signal. Green signal for RGB CRT display.
69	O	D3B1	Video signal. Blue signal for RGB CRT display.
70	O	D4I1	Video signal. Intensity signal for ~~RGB~~ CRT
71	I	CHFONT0	Change character font signal.
72	I	FLTDSL1	Flat display selected. It changes internal /external display.
73	I	OSC171	Clock 17.5 MHz.
74	O	CEH0	Chip enable high. chip selected signal for the V-RAM.

Interface Signal (Continued)

Pin	I/O	Signal Name	Description
75	O	WRCC0	Write character code. It is used with chip enable signal to write the V-RAM. (evven address)
76	O	WRAT0	Write attribute data. It is used with chip enable signal to write the V-RAM. (odd address)
77	O	CEL0	Chip enable low. It is V-RAM selection signal.
78		Vcc	+5v
79	O	URA001	CPU/Refresh address bit 0.
80	O	URA011	CPU/Refresh address bit 1.
81	O	URA021	CPU/Refresh address bit 2.
82	O	URA031	CPU/Refresh address bit 3.
83	O	URA041	CPU/Refresh address bit 4.
84	I/O	AT01	Attribute data bit 0.
85	I/O	AT11	Attribute data bit 1.
86	I/O	AT21	Attribute data bit 2.
87	I/O	AT31	Attribute data bit 3
88	I/O	AT41	Attribute data bit 4.
89	I/O	AT51	Attribute data bit 5.
90	I/O	GND	Ground
91	I/O	AT61	Attribute data bit 6.
92	I/O	AT71	Attribute data bit 7.
93	I/O	CC01	Character code data bit 0.
94	I/O	CC11	Character code data bit 1.
95	I/O	CC21	Character code data bit 2.
96	I/O	CC31	Character code data bit 3.
97	I/O	CC41	Character code data bit 4.
98	I/O	CC51	Character code data bit 5.
99	I/O	CC61	Character code data bit 6.
100	I/O	CC71	Character code data bit 7.

Display Controller Subsystem

Display Controller Subsystem (DCS) is composed of following components.

Table C-1

Display Controller GA		CMOS 5 KG 100-pin flat Package
Video-RAM		32 KB 64 K SRAMx4
CG-ROM		32 KB 256 K ROMx1
OSC	CPU-CLK	14.31818 MHz
	Other	17.5 MHz
Others	Multiplexer Latch Display Buffer	74HC157x2 74HC273x1

Generally B stands for Byte, and b for bits.

Table C-2 is the operation mode of the DCS of internal plasma/LCD display and external CRT display.

Table C-2

Operation Mode	Plasma (Pixels)		LCD/ ~~External~~ CRT(Pixels)	
	Resolution	Character Box	Resolusion	Character Box
40x25 TEXT	320x400	8x16	320x200	8x8
80x25 TEXT	640x400	8x16	640x200	8x8
320x200 GRAPH	320x200	8x8	320x200	8x8
640x200 GRAPH	640x200	8x8	640x200	8x8
640x400 GRAPH	640x400	8x16	not supported	

Signals

The DCS has follwing groups of signals.

- o I/O Interface Signals (23 lines)
- o V-RAM Signals (34 lines)
- o Character Generator (CG) Signals (16 lines)
- o Video Signals (9 lines)
- o Display Mode Select Signals (3 lines)
- o Clock Input (2 lines)
- o Miscellaneous Signals (5 lines)

1) I/O Interface Signals (23 lines)

DIOSL0 : Display I/O Select (Input)
This signal allows the CPU to read or write data from/to I/O port within the GA when this signal is low.
IORD10 or IOWR10 should be low as well as DIOSL0 for read or write operation to I/O port within the GA.

IORD10 : I/O Read (Input)
I/O port data within the GA is transferred to the CPU through the SYD71-SYD01 when this signal is low and DIOSL0 is low too.

IOWR10 : I/O Write (Input)
Data from the CPU is transferred and written to the selected I/O port within the GA through the SYD71-SYD01 when this signal is low and DIOSL0 is low too.

DMESL0 : Display Memory Selected (Input)
This signal allows the CPU to read or write data from/to the Video RAM when this signal is low.
MRD0 or MWR0 should be low as well as DMESL0 for read or write operation to V-RAM.

MRD0 : Memory Read (Input)
Read operation to the V-RAM is executed and read data is transferred to the SYD7l-SYD0l when this signal is low and DMESL0 is low too.

MWR0 : Memory Write (Input)
Data from the SYD7l-SYD0l is written to the V-RAM when this signal is low and DMESL0 is low too.

A05l-A0ll,A0Bl,Al4l : CPU Address (Input)
These are address data lines from the CPU or DMAC and high level is logical true.
A03l-A0ll and A0Bl are used for selecting one of I/O ports within the GA during read or write operation to the I/O port within the GA.
For memory read or memory write operation to the V-RAM, A05l-A0ll,A0Bl and Al4l go through the GA then they are used to selecting memory location of the V-RAM with Al3l-A06l.

SYD7l-SYD0l : 8-bit Data Bus (Input/Output)
These are 8-bit data lines and high level is logical true.
The data is go through these lines while read/write operation to the I/O port within the GA or read/write operation to the V-RAM.

IORDYl : I/O Ready (Output)
It is ready when this line is high level. If DMESL0 is low (the CPU or DMAC requests V-RAM access), the GA holds this line low level to make the CPU or DMAC to waite until the end of the access. This signal line is held high level usually and it is also high when the CPU reads or writes data from/to the I/O port within the GA.

RESET0 : Reset (Input)
The GA is reset when this signal line is low level.

2) V-RAM Signals (34 lines)

URA04l-URA00l : CPU/Refresh Address 00 - 04 (Input)

These lines used to send a part of CPU address and a part of refresh address to the V-RAM.
The CPU address is from CPU address lines A05l-A01l.

RA12l-RA05l : Refresh Address 05 - 12 (Input)

These lines are address lines for the V-RAM refreshment.
RA12l-RA06l as high-order bits of address lines are input to the D-RAM through the multiplexer which has another input of I/O bus address (A13l-A06l), while URA04l-URA00l are directly connected input pins of the V-RAM. (see Fig x-1)
There are two ways to read or write data from/to the V-RAM. One way is that the CPU reads or writes it from/to the D-RAM through the I/O bus. The other is Display refresh (read only) by the GA.
The addressing of the each case is shown on the Table x-1.

CEL0,CEH0 : Chip Enable Low/High (Output)

These signals are chip-enable signals of the V-RAM, and they are active when low. The block diagram of the V-RAM control signals and logical operation of the signals are shown respecively on the Fig. x-2 and Table x-2. The V-RAM is composed of four 8Kx8bit SRAM (TC5565). CEL0 address 16KB of two S-RAMs starting from B8000h, and CEH0 addresses 16KB of two S-RAMs starting from BC000h respectively.
The RAMs connected to the data bus of CC7l-CC0l are assigned to even address and the RAMs connected to the data bus of AT7l-AT0l are assigned to odd address respectively. For V-RAM refresh, two byte read operation is done always. Whenever the CPU and DMAC reads the data stored in the V-RAM, two RAMs (two bytes) are accessed simultaneously, although only one of the two can be put on the data lines (SYD7l-SYD0l) of the I/O bus. CC7l-CC0l are read out to the I/O bus SYD7l-SYD0l if A0Bl is low, and AT7l-AT0l are read out to the I/O bus SYD7l-SYD0l if A0Bl is high. Two RAMs (CC7l-CC0l and AT7l-AT0l) become to be enable but only one RAM is written when the CPU or DMAC executes write operation.

WRCC0 : Write Character Code (Output)
WRAT0 : Write Attribute Data (Output)

They are write enable signal to the V-RAM.
Write operation into V-RAM is enabled when chip enable signal and one of WRCC0/WRAT0 to the V-RAM chip are low. It is also executed only when the CPU or DMAC request to write (DMESL0=low and MWR0=low). At this point, one of WRCC0 and WRAT0 becomes low according to the A0Bl state. WRCC0 becomes low when A0Bl is low, and write data on the I/O bus SYD7l-SYD0l is transferred to CC7l-CC0l. WRAT0 becomes low when A0Bl is low, and write data on the I/O bus SYD7l-SYD0l is transferred to AT7l-AT0l.

Table C-3

V-RAM		CPU Address	Memory Refresh	
Pin Name	Signal Name		TEXT Mode	GRAPH Mode
$\overline{CE}$	CEH0/CEL0	A14	MA13	RSA1
AD12	RA121	A13	MA12	RSA0
AD11	RA111	A12	MA11	MA11
AD10	RA101	A11	MA10	MA10
AD09	RA091	A10	MA09	MA09
AD08	RA081	A09	MA08	MA08
AD07	RA071	A08	MA07	MA07
AD06	RA061	A07	MA06	MA06
AD05	RA051	A06	MA05	MA05
AD04	RA041	A05	MA04	MA04
AD03	RA031	A04	MA03	MA03
AD02	RA021	A03	MA02	MA02
AD01	RA011	A02	MA01	MA01
AD00	RA001	A01	MA00	MA00
$\overline{WE}$	WRCC0/WRAT0	A00	--	--

Note:

* A141-A001 are I/O bus address lines from the CPU.
  A051-A001 and A141 are input to CPU address input pins of the GA.

* MA13-MA00 are Refresh Memory Address.
  They are generated by the 6845 compatible circuit within the GA.

* RSA1-RSA0 are Raster Scan Address.
  There are four Raster Scan Address lines ((RSA3(MSB) - RSA0(LSB)), but only two lower-bits are used in graphics mode.

Figure C-2 V-RAM Control Signals

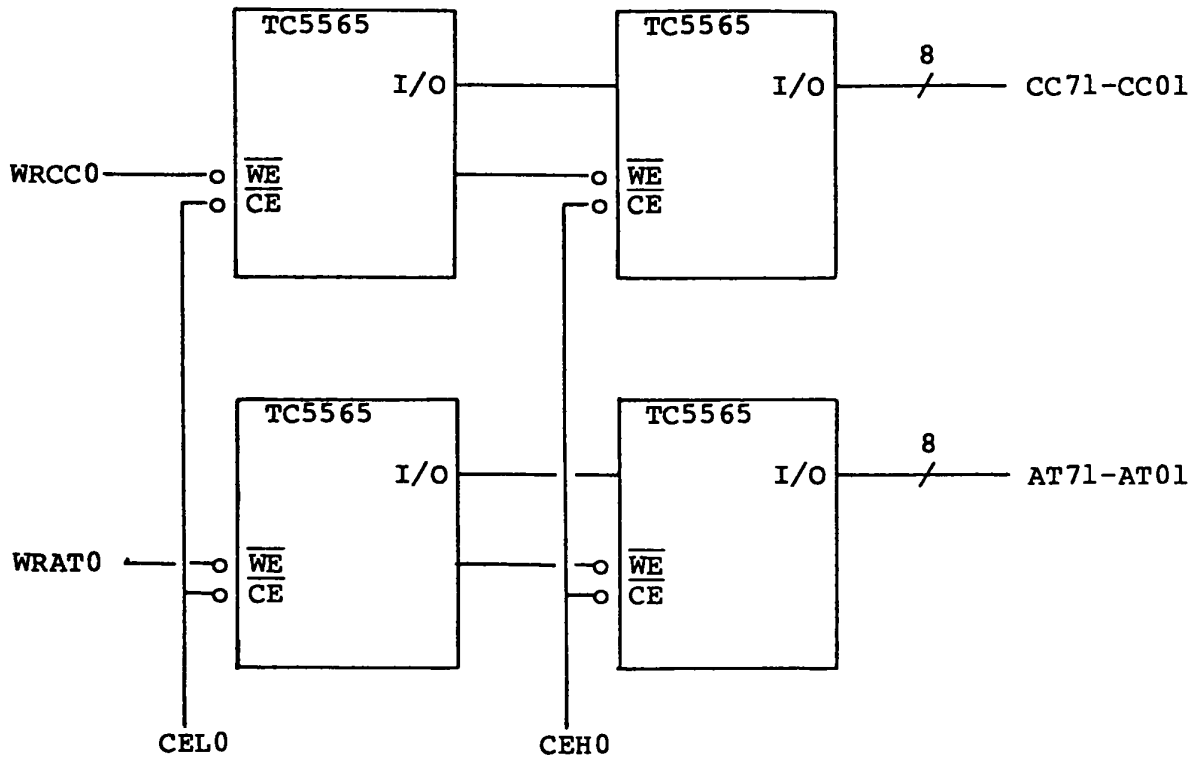


Table C-4 V-RAM Control Signals

V-RAM Control Signal	CPU Address		Display Refresh
	Read	Write	
CEL0	if A141=low, Low	if A141=low, Low	if MA131 or RSA1 =Low, Low
CEH0	if A141=high, Low	if A141=high, Low	if MA131 or RSA1 =High, Low
WRCC0	High	if A0B1=Low, Low	High
WRAT0	High	if A0B1=High, Low	High

RASEL0 : Refresh Address Selection (Output)
This signal is an input selection signal to the V-RAM address multiplexer. If it is low, the display refresh address lines (RA12-RA05) are selected as V-RAM address. If it is high, the I/O bus address lines are selected as V-RAM address.

CC7 - CC0 : Character Code Data Bus (Input/Output)
These lines are data bus from/to the even address V-RAM.
The even address V-RAM is used to store the character codes in TEXT mode.

AT7 - AT0 : Attribute Data Bus (Input/Output)
These lines are data bus from/to the odd address V-RAM.
The even address V-RAM is used to store the attribute codes in TEXT mode.

3) Character Generator (CG) Signals (16 lines)

CGAX1 : CG Address Latch (Output)
The character code from the V-RAM (CC7-CC0) is set to the external latch circuit by this signal. The set timing of the external latch circuit is at the raising edge of this signal. The output from the external latch circuit is used for the address of CG-ROM. The character code is 8-bit code, and it can selects one of 256 characters.

ROM Address (Output)
Following 6 signals are also used as CG-ROM address as well as the character code mentioned above.

CGM0 : Plasma Font Selection.
INTEN1 : Intensified Font Selection.
RSA3-RSA0 : Raster Scan Address.

Table x-3 and Figure x-3 shows ROM address assignment.
CG-ROM (32 KB) has following character fonts.

8x8 single dot character set
8x8 double dot character set
8x16 single dot character set
8x16 double dot character set

The plasma display can not display intensified character like CRT display, thus double dot character is used for distinction between normal character and intensified character.
INTEN1 signal is used to select single or double dot character.
    INTEN1=Low --- Single dot character.
    INTEN1=High -- Double dot character.

CGM01 signal is used to select 8x16 or 8x8 character font.
    CGM01=Low --- 8x16 character.
    CGM01=High -- 8x8 character.

RSA21-RSA01 and RSA31 are Raster Scan Address. The RSA01 is the Least Significant Bit (LSB).

CEROM0 : Chip Enable for ROM (Output)
It makes the CG-ROM to be enable for access.

CG71 - CG01 : Character Generator Output Signals (Output)
These lines are output signals of the CG-ROM.
The data addressed by ROM address is read out to the CG71-CG01 lines, when CEROM0=0.

RSA31	RSA21	RSA11	RSA01	Raster
H	L	L	L	0
H	L	L	H	1
H	L	H	L	2
H	L	H	H	3
H	H	L	L	4
H	H	L	H	5
H	H	H	L	6
H	H	H	H	7

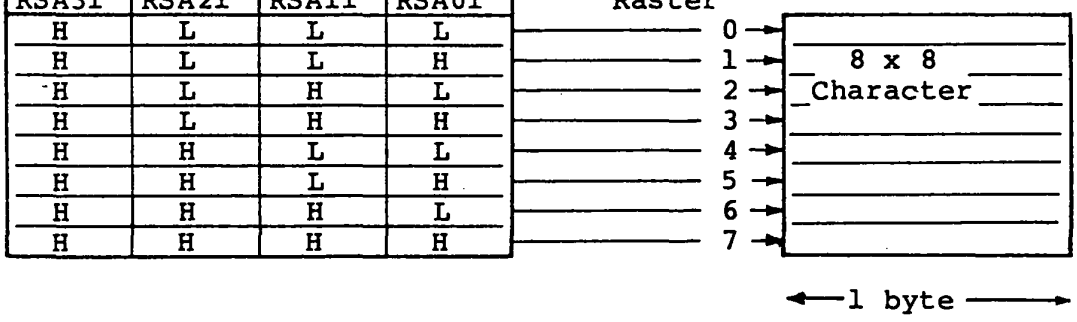


Figure C-3 ROM Address Assignment

RSA31	RSA21	RSA11	RSA01	Raster
H	L	L	L	0
H	L	L	H	1
H	L	H	L	2
H	L	H	H	3
H	H	L	L	4
H	H	L	H	5
H	H	H	L	6
H	H	H	H	7
L	L	L	L	8
L	L	L	H	9
L	L	H	L	10
L	L	H	H	11
L	H	L	L	12
L	H	L	H	13
L	H	H	L	14
L	H	H	H	15

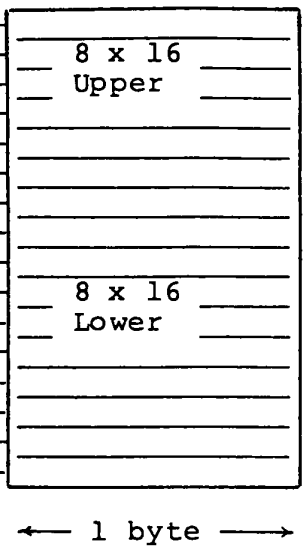


Table C-5 ROM Address Assignment

ROM Add.Pin	GA Signal
AD14	+VCC
AD13	CGM01
AD12	RSA31
AD11	INTEN1
AD10	CC71
AD09	CC61
AD08	CC51
AD07	CC41
AD06	CC31
AD05	CC21
AD04	CC11
AD03	CC01
AD02	RSA21
AD01	RSA11
AD00	RSA01

	32 KB - ROM
4000h	8x16 Single Dot Lower Half
4800h	8x16 Double Dot Lower Half
5000h	8x16 Single Dot Upper Half
5800h	8x16 Double Dot Upper Half
6000h	———
6800h	———
7000h	8x8 Single Dot
7800h	8x8 Double Dot
7FFFh	

Note: Addresses 0h-3FFFh of CG-ROM are not used.

4) Video Signals (9 lines)

There are 9 video signals which are output from the GA.
They are sent to the plasma display or external CRT display.
The signals are used in the each unit as shown Table C-6.

Table C-6 Video Signals

GA Signal	Plasma Display	CRT Display	
		RGB	Composite
LPHS1	PHSY0	CHSY1	
FPVS1	PVSY0	CVSY1	
FRHV1			CHVSY0
D1R1	PD10	CRV1	
D2G1	PD20	CGV1	
D3B1	PD30	CBV1	
D4I1	PD40	CIV1	CIV1
SXVD1	PSCK0		CVD1
BFR0			CBLNK0

5) Display Mode Selection Signals (3 lines)

CHFONT0 : Character Font Change (Input)
This signal is to change the font desplayed on the screen.
The function of this signal is shown on the Table C-7.

FLTDSL1 : Flat Display Selected (Input)
This signal is to select one of internal and external display unit.
If this signal is high level, the internal plasma display is selected.
If this signal is low level, the external CRT display (RGB, Composite) is selected.

PDP0 : Plasma Display Panel (Input)
This signal is to specify the type of internal display unit.
If this signal is low level, a plasma display unit (640x400 pixels) is used as internal display unit.
If this signal is high level, a LCD display unit (640x200 pixels) is used as internal display unit.

Note: Relation between signals of CHFONT0,FLTDSL1,PDP0 and character fonts on the screen are shown on the Table C-7.

Table C-7

Mode	bit 3 of attribute byte	GA Input			GA Output		Selected Display	Selected Display
		CHFONT0	FLTDSL1	PDP0	INTEN1	CGM01	Display	Display
80x25 or 40x25	0	H	H	H	H	H	LCD	8x8 Double
	1	H	H	H	L	H	LCD	8x8 Single
	0	L	H	H	L	H	LCD	8x8 Single
	1	L	H	H	H	H	LCD	8x8 Double
80x25 or 40x25	0	H	H	L	L	L	Plasma	8x16 Single
	1	H	H	L	H	L	Plasma	8x16 Double
	0	L	H	L	H	L	Plasma	8x16 Double
	1	L	H	L	L	L	Plasma	8x16 Single
80x25 or 40x25	0	H	L	x	H	H	CRT	8x8 Double
	1	H	L	x	H	H	CRT	8x8 Double (High Light)
	0	L	L	x	L	H	CRT	8x8 Single
	1	L	L	x	L	H	CRT	8x8 Single (High Light)

6) Clock Input (2 lines)

OSC14I : Oscillator 14 MHz (Input)
This clock is the input signal to generate a video signal for the CRT display. The frequency of the clock must be 14.31818 MHz.

OSC17I : Oscillator 18 MHz (Input)
This clock is the input signal to generate a video signal for the plasma display. The frequency of the clock must be 17.5 MHz (60 Hz).

7) Miscellaneous Signals (5 lines)

GOFI : GA Off (Input)
It forces the GA to be disable if this signal is high. It forces the GA to be disable when the other display adaptor is installed in the I/O expansion box and the external display adaptor is used.

SBEI : SBE-LCD (Input)
This signal is reserved for LCD display.

TOSHIBA

LOGIC DIAGRAM

TI100 PLUS

CPU0195

変更回数 REV. MARK	記事 CONTENTS	承認 APPROVED BY	担当 REVISED BY	保管 REGISTERED
AO	発行 ISSUE	. .	A. Kaneko '86.6.3	. .
B	FPLUS 2 用に変更 (Changed to FPLUS2)	T. Yamazaki June.3 '86	A. Kaneko 86.6.3	. .
		. .	. .	. .
		. .	. .	. .
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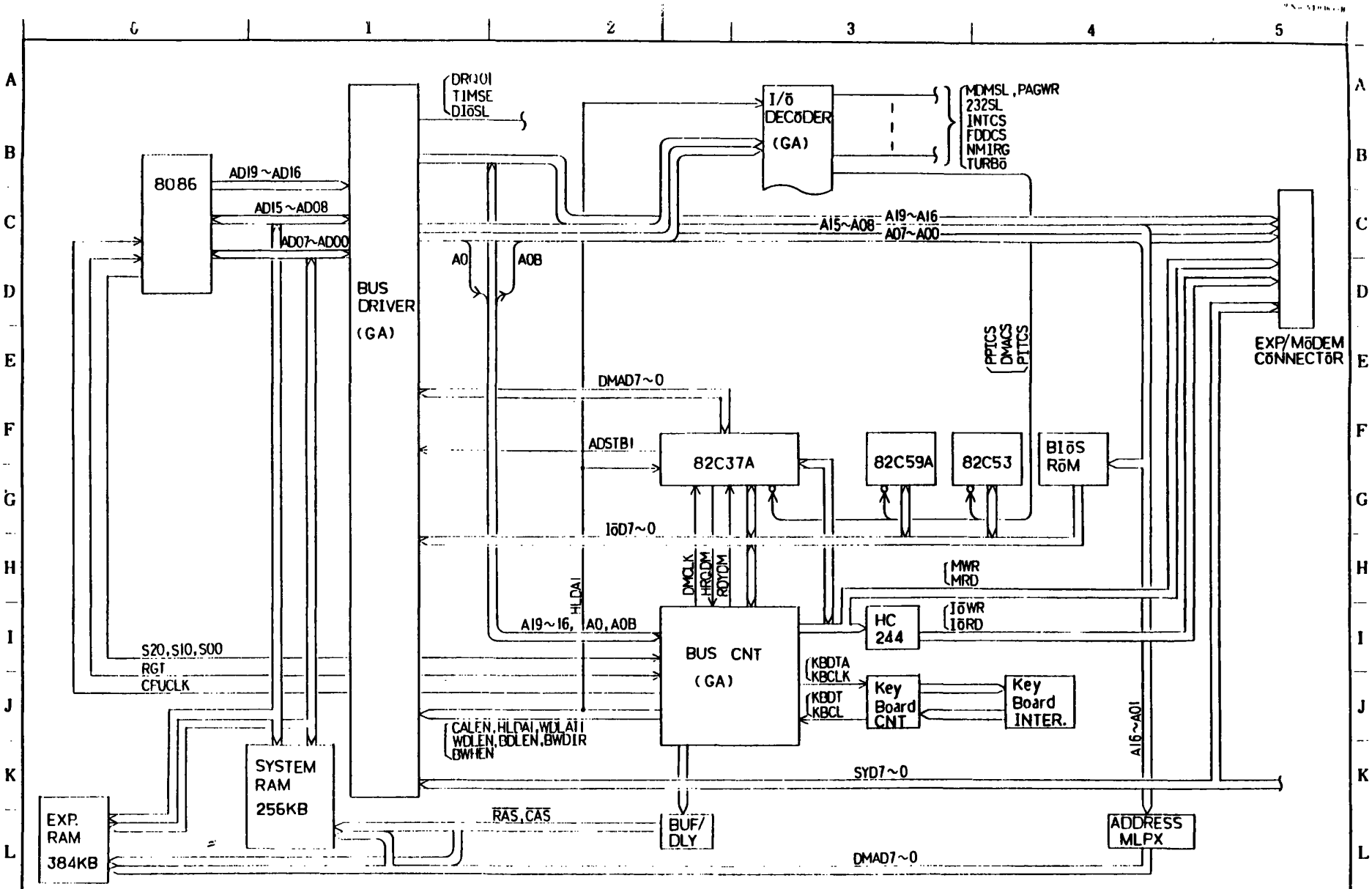
		. .	. .	. .

株式会社 東芝
TOSHIBA CORPORATION

ML (有・無)

承認 APPROVED BY	検図 CHECKED BY	設計 DESIGNED BY	製図 DRAWN BY	図面番号 DRAWING NO.
T. Yamazaki June.3 '86	. .	A. Kaneko '86.6.3	. .	72M14 0015
保管 REGISTERED	. .			TOTAL 30 CONT. ON 2 PAGE NO. 1



REVISED BY	REVISED DATE	PRINTED BOARD	TITLE : BLOCK DIAGRAM I	
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No.	DRAWING No.	PAGE No. 2	REV MARK

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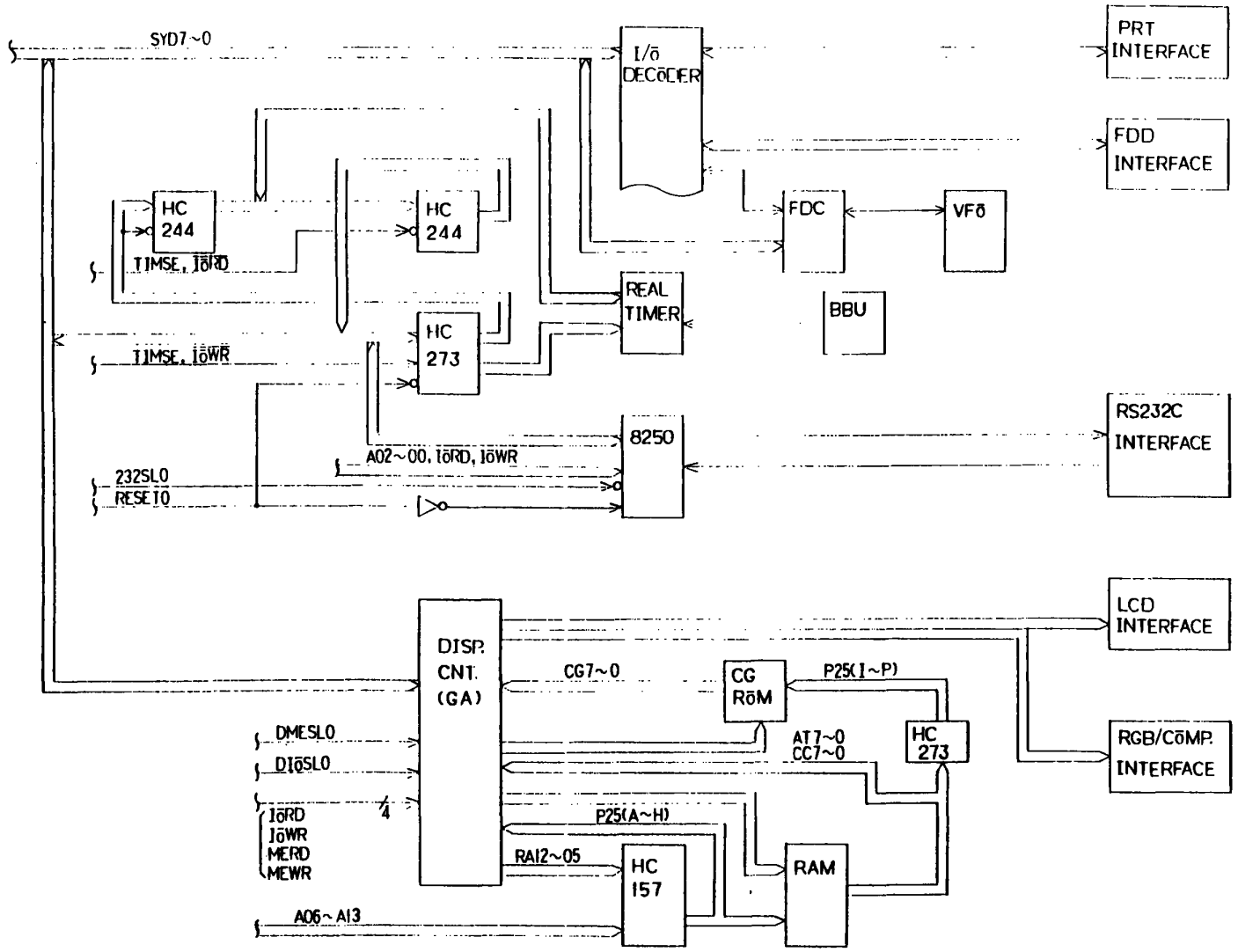

REVISED BY	REVISED DATE	PRINTED BOARD	TITLE: BLOCK DIAGRAM II		
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No.	DRAWING No.	PAGE No. 3	REV. MARK

PJ 16 EXP. BUS

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	GND		17	02	Vcc		17
03	M9VDC			01	P9VDC		
05	MEMSL0			06	C0MCLK1		
07	MIRQ0			08	SPK1$\bar{0}$N0		
09	GND			10	AA0B1		
11	A011			12	A021		
13	A031			11	A041		
15	A051			16	A061		
17	A071			18	GND		
19	A081			20	A091		
21	A101			22	A111		
23	A121			21	A131		
25	A141			26	A151		
27	GND			28	A161		
29	A171			30	A181		
31	A191			32	SYD01		
33	SYD11			31	D21		
35	D31			36	GND		
37	D41			38	SYD51		
39	D61			10	D71		
11	MWR0			12	MRD0		
13	GND			11	I$\bar{0}$WR20		
15	I$\bar{0}$RD20			16	TC1		
17	CALEN1			18	RSET1		
19	DACK10			50	IRQ21		
51	GND			52	Vcc		
53	CPUCK11			54	IRQ51		
55	DRQ31			56	DACK30		
57	CPADE0			58	DRQ11		
59	I$\bar{0}$RDY1			60	EXPAN0		

PJ13 RGB

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	GND		23	02	GND		23
03	CRV1			04	CGV1		
05	CBV1			06	CIV1		
07	NC			08	CHSY1		
09	CVSY1			10			

PJ3

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	BFR0		23	02	FRHV1		23

PJ 9 EXP. MEM

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	MEM0		6	02	Vcc		6
03	MAD81			01	MAD71		
05	MAD61			06	MAD51		
07	MAD41			08	MAD31		
09	GND			10	MAD21		
11	MAD11			12	MAD01		
13	MDPH1			11	MDPL1		
15	AD151			16	AD141		
17	GND			18	AD131		
19	AD121			20	AD111		
21	AD101			22	AD091		
23	AD081			21	AD071		
25	GND			26	AD061		
27	AD051			28	AD041		
29	AD031			30	AD021		
31	AD011			32	AD001		
33	GND			31	MWE0		
35	RAS20			36	RAS30		
37	PRAS0			38	CASH0		
39	RAS40			10	CASL0		
11				12			
13				11			

PJ 8 LED

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	FAST1		9	02	Vcc		9
03	SELA0			01	SELB0		
05	L$\bar{0}$WBT0			06	L$\bar{0}$WSP1		
07	CRTM0			08	FT$\bar{0}$F0		
09	GND			10			

PJ10 PS

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	P9VDC		25	02	M9VDC		25
03	M14VDC			04	GND		
05	LCDSL1			06	L$\bar{0}$WBT0		
07	DM$\bar{0}$NAB1			08	EXPAN0		
09	MEM0			10			

PJ 6 FDD A

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	Vcc		14	02	IND0		15
03				01	DSELA0		14
05				06	DSKC0		15
07				08	RDY0		
09				10	M$\bar{0}$NA0		14
11	NC			12	DIRC0		
13	GND			11	STEP0		
15				16	WRDA0		
17				18	WGATO		
19				20	TR00		15
21				22	WPR0		
23				21	RDA0		
25				26	SIDE0		14

PJ4 SPK

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	SP$\bar{0}$T01		5	02	SP$\bar{0}$T11		5

PJ 7 FDD B

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	Vcc		14	02	IND0		15
03				01	DSELB0		14
05				06	DSKC0		15
07				08	RDY0		
09				10	M$\bar{0}$NB0		14
11	NC			12	DIRC0		
13	GND			11	STEP0		
15				16	WRDA0		
17				18	WGATO		
19				20	TR00		15
21				22	WPR0		
23				24	RDA0		
25				26	SIDE0		14

PJ12 C0MP.

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	P26CP		24	03	GND		24

REVISED BY	REVISED DATE	PRINTED BOARD	TITLE: CONNECTOR PIN SIGNAL MAP I	
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No.	DRAWING No.	PAGE No. 4	REV MARK

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PJ 14 PRT/FDD

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	STRŌBO		16	02	PD01		16
03	FD11			01	21		
05	31			06	41		
07	51			08	61		
09	71			10	ACK0		
11	BUSY0			12	PE1		
13	SELEC1			11	AUTFD0		
15	ERRŌR0			16	PINT0		
17	SLIN0			18	GND		
19	GND			20			
21				22			
23				21			
25				26			
27				28			
29				30			
31				32			
33				31			
35				36			
37				38			
39				10			
11				12			
13				11			
15				16			
17				18			
19				50			

PJ 1 KB

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	KBŌT00		8	02	KBŌT01		8
03	02			01	GND		
05	03			06	KBŌT04		
07	05			08	06		
09	GND			10	07		
11	KBŌT08			12	09		
13	10			11	KBRT00		
15	KBRT10			16	20		
17	30			18	GND		
19	40			20	KBRT50		
21	60			22	70		
23				21			
25				26			
27				28			
29				30			
31				32			
33				31			
35				36			
37				38			
39				10			
11				12			
13				11			

PJ 2 LCD

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	GND		23	02	PFRHV1		23
03	PVSYD			01	PHSYD		
05	PSCK0			06	GND		
07	PD40			08	PD30		
09	20			10	10		
11	GND			12	LCDP5V		
13	CNTRST1			11	M14VDC		
15	GND			16			
17				18			
19				20			
21				22			
23				21			
25				26			

PJ17

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	Vcc		22	02	P25A121		22

PJ18

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	Vcc		22	02	P25A141		22

PJ 19

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	LŌWBT0		24	02	P26IV1		24
03				01			
05				06			
07				08			

PJ 15 RS232C

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	DCD1		19	02	RD0		19
03	SD0			01	DTR1		
05	GND			06	DSR1		
07	RTS1			08	CTS1		
09	RI1			10			
11				12			
13				11			
15				16			
17				18			
19				20			

REVISED BY	REVISED DATE	PRINTED BOARD	TITLE: CONNECTOR PIN SIGNAL MAP II	
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No.	DRAWING No.	PAGE No. 5	REV. MARK

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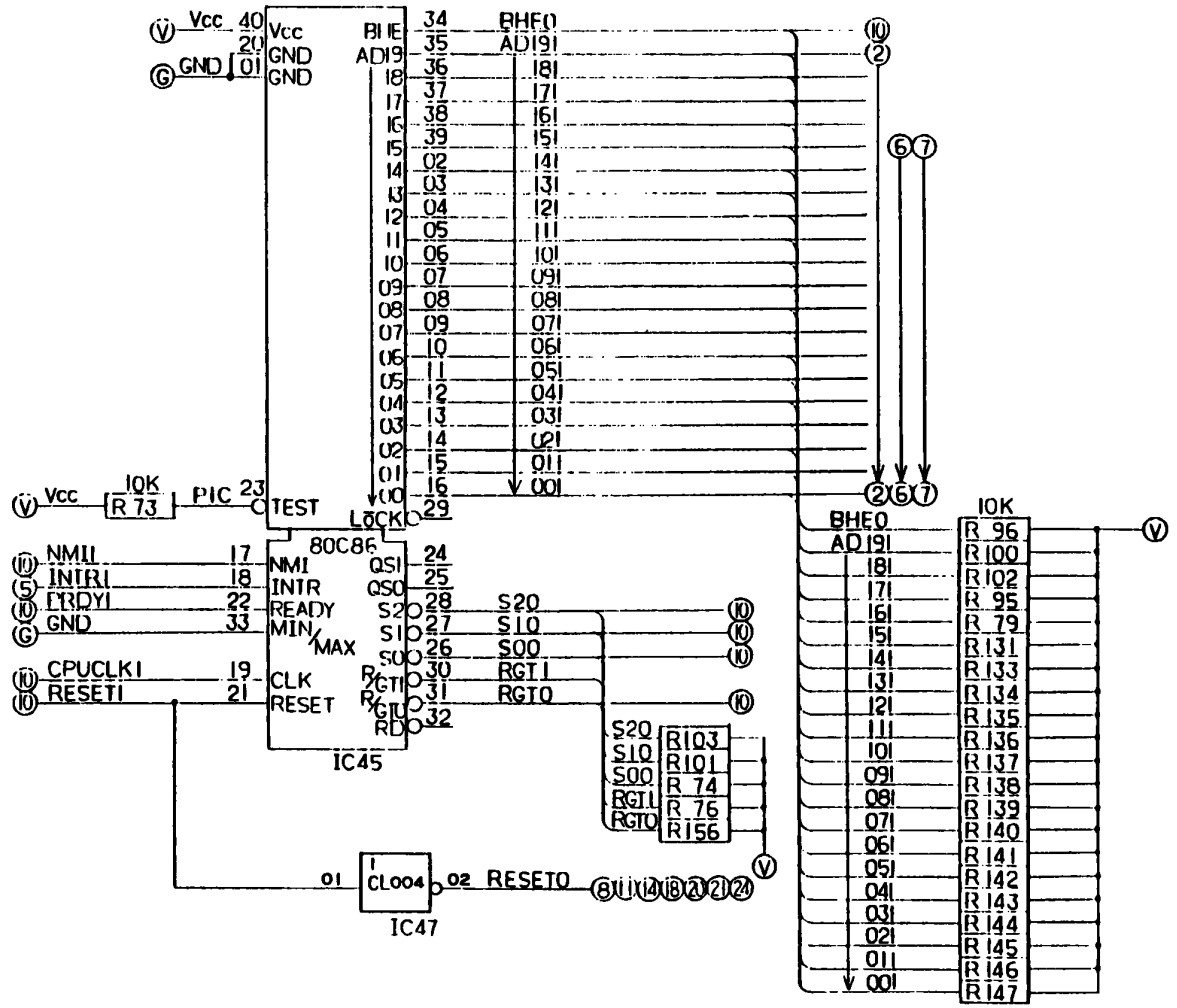

REVISED BY	REVISED DATE	PRINTED BOARD	TITLE: PROCESSOR		
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 1	DRAWING No	PAGE No. 6 / REV. MARK

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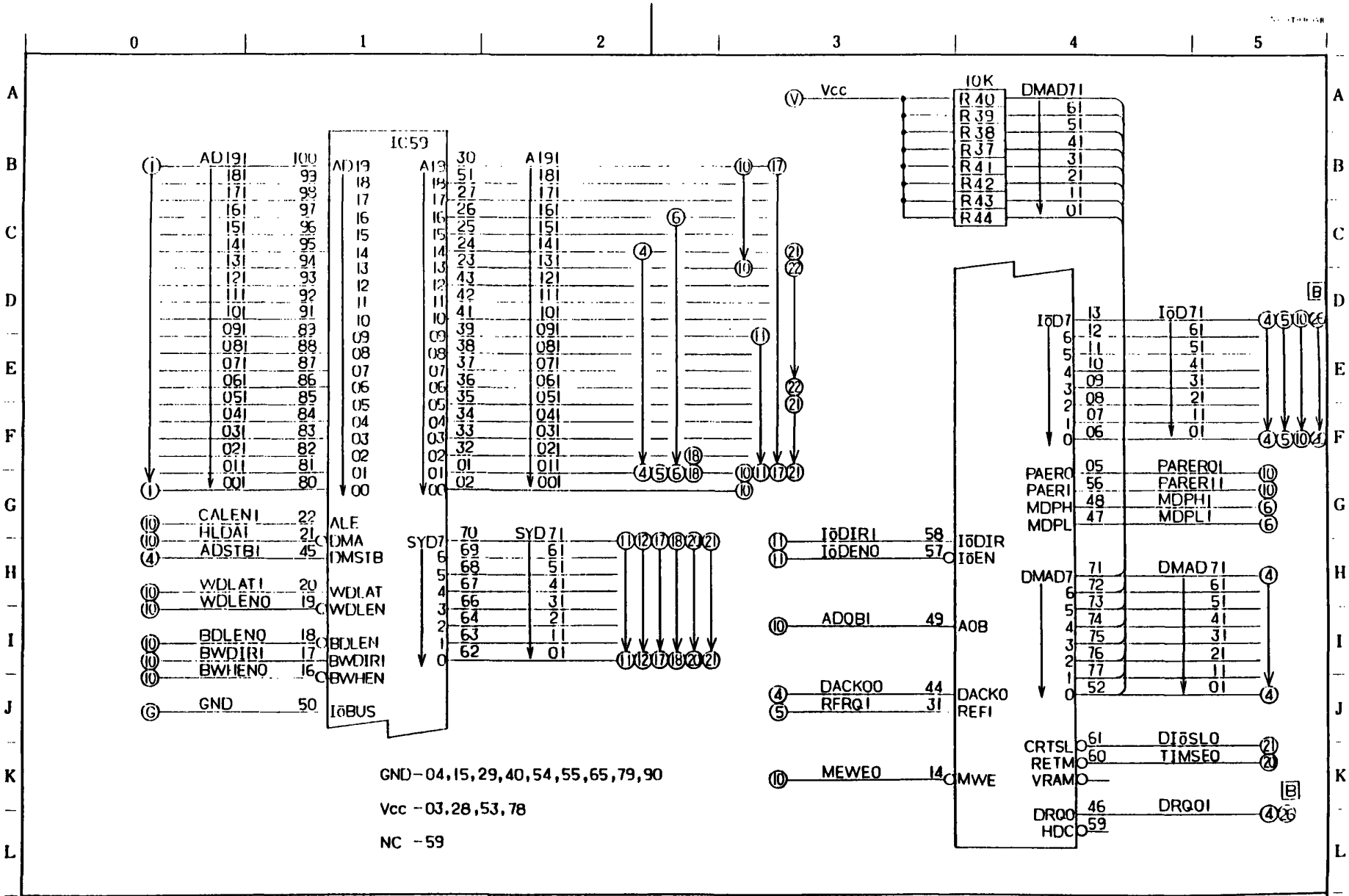

REVISED BY	REVISED DATE	PRINTED BOARD	TITLE: BUS DRIVER		
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 2	DRAWING No.	PAGE No. 7 / REV. MARK

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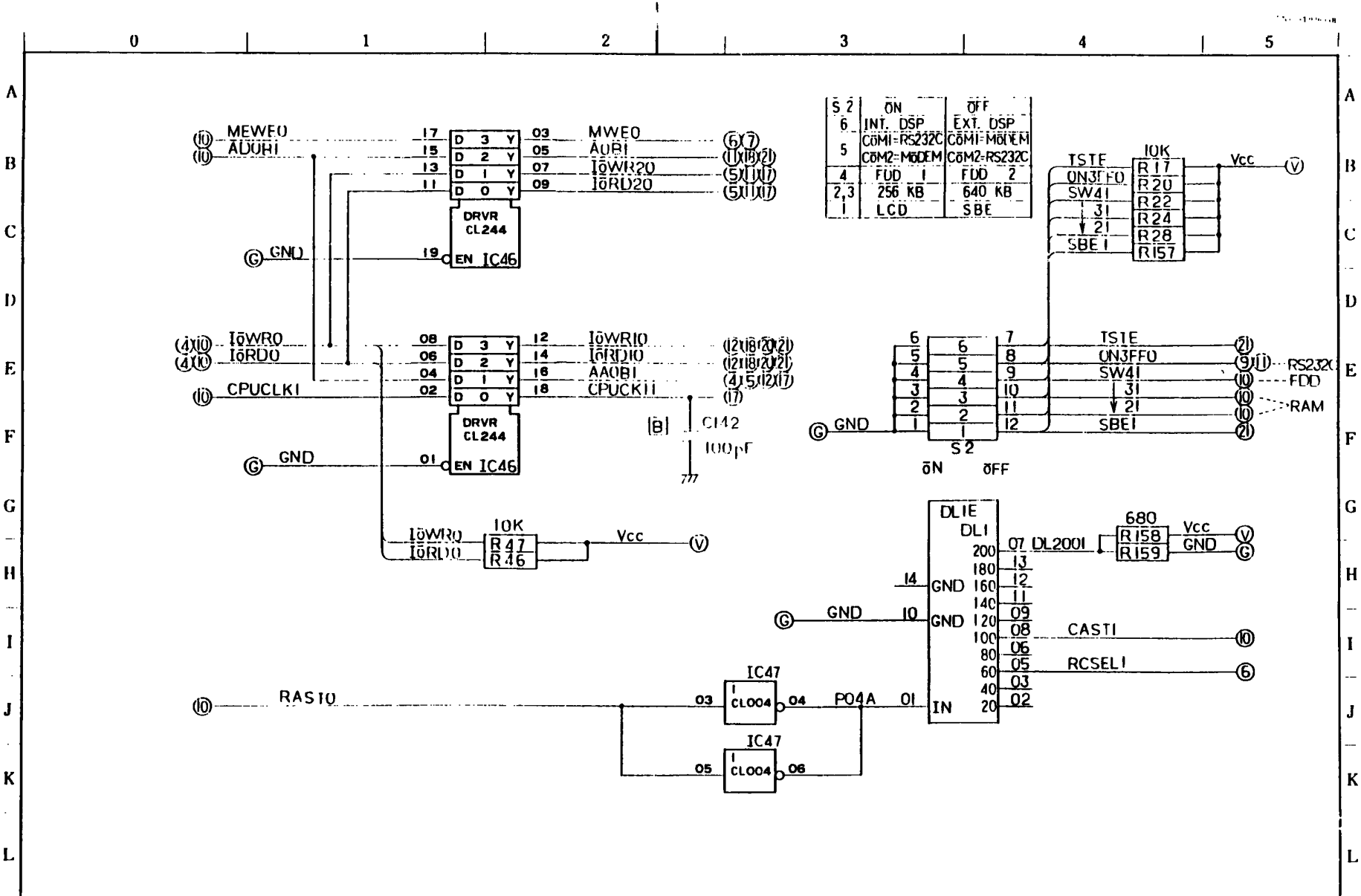

REVISED BY	REVISED DATE	PRINTED BOARD	TITLE : COMMAND DRIVER , SW and DL		
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No. 3	DRAWING No.	PAGE No. 8 / REV. MARK

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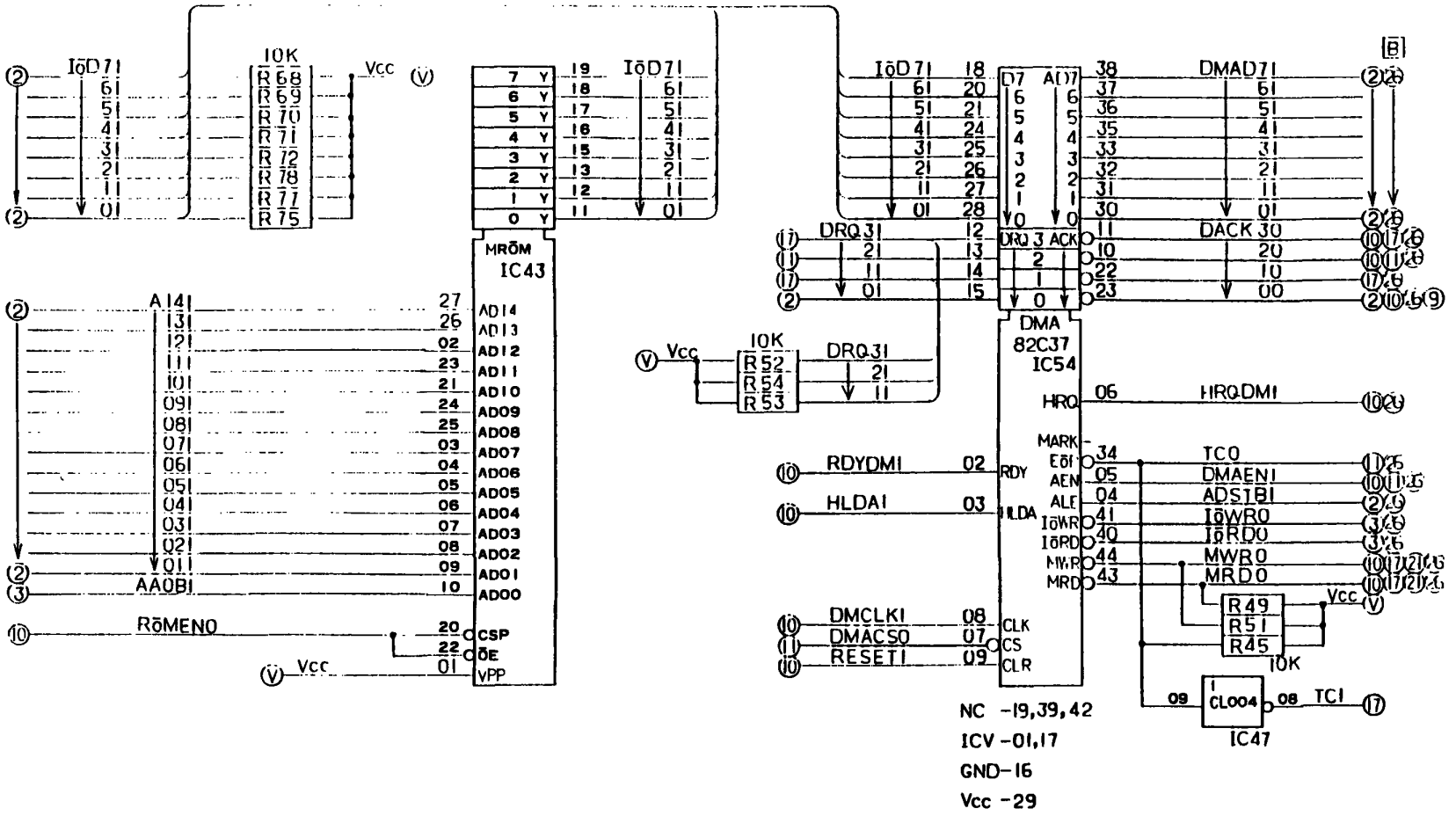
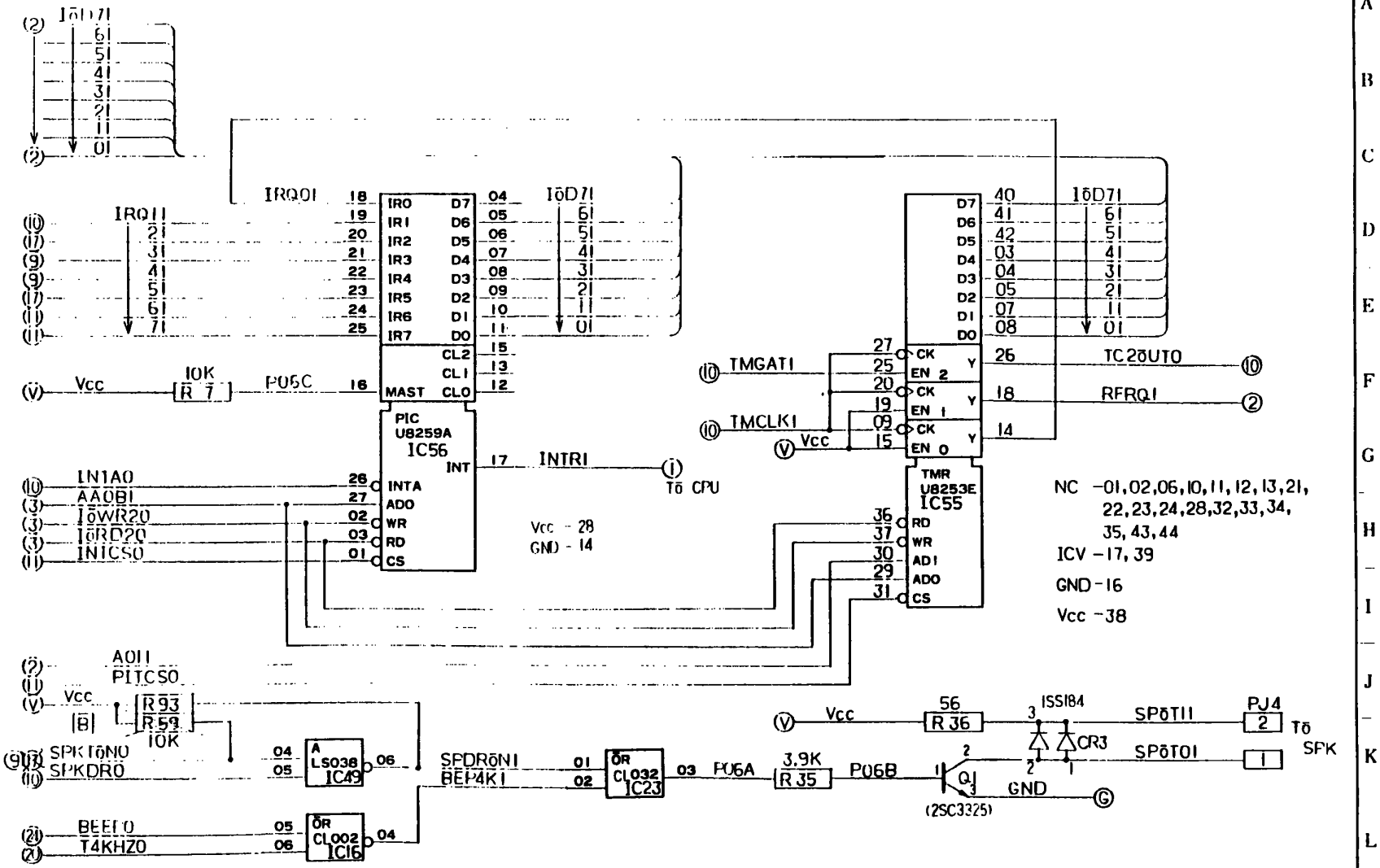
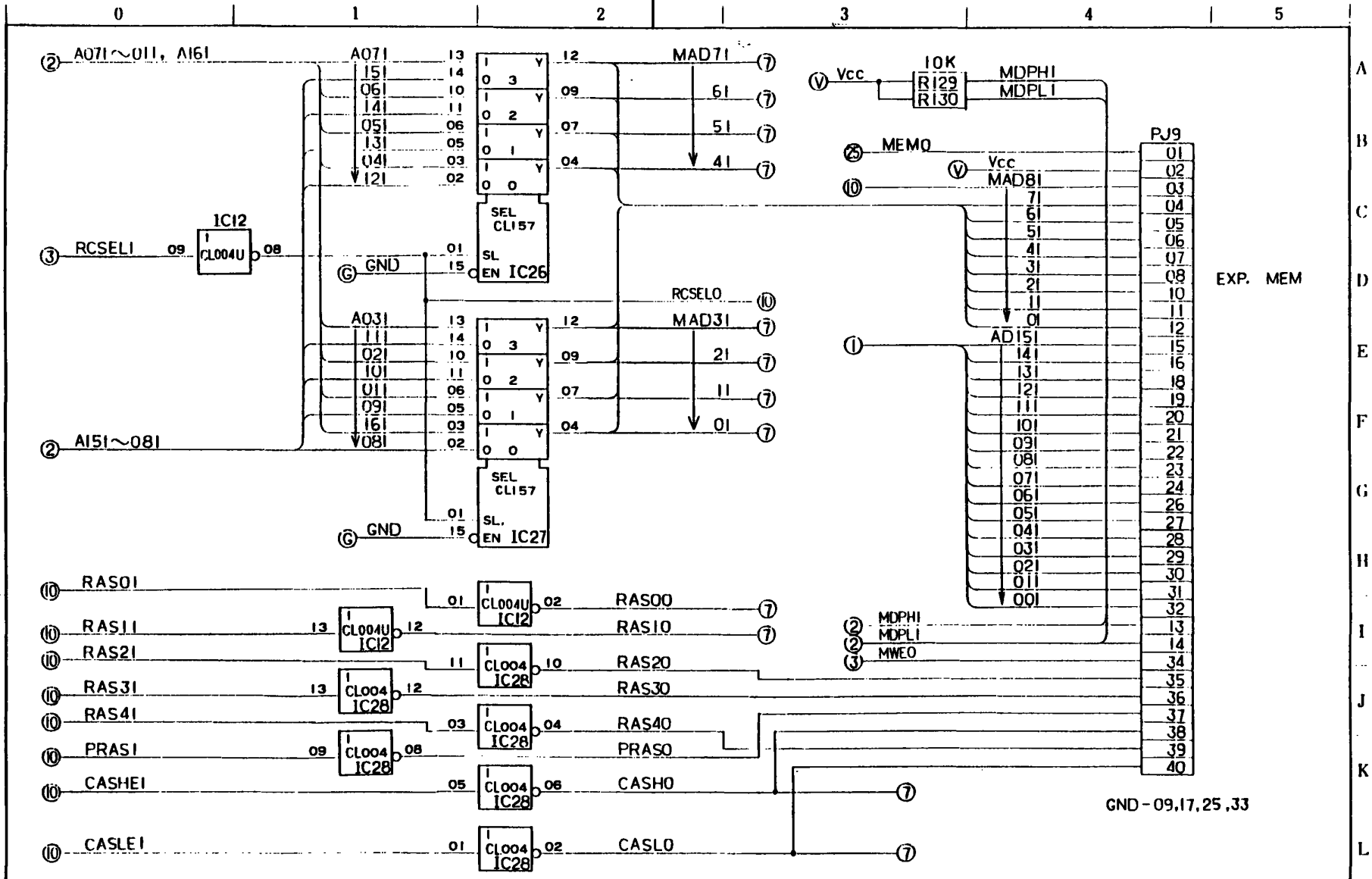


REVISED BY	REVISED DATE	PRINTED BOARD	TITLE				
			RŌM and DMAC				
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No. 4	DRAWING No.	PAGE No. 9	REV. MARK	



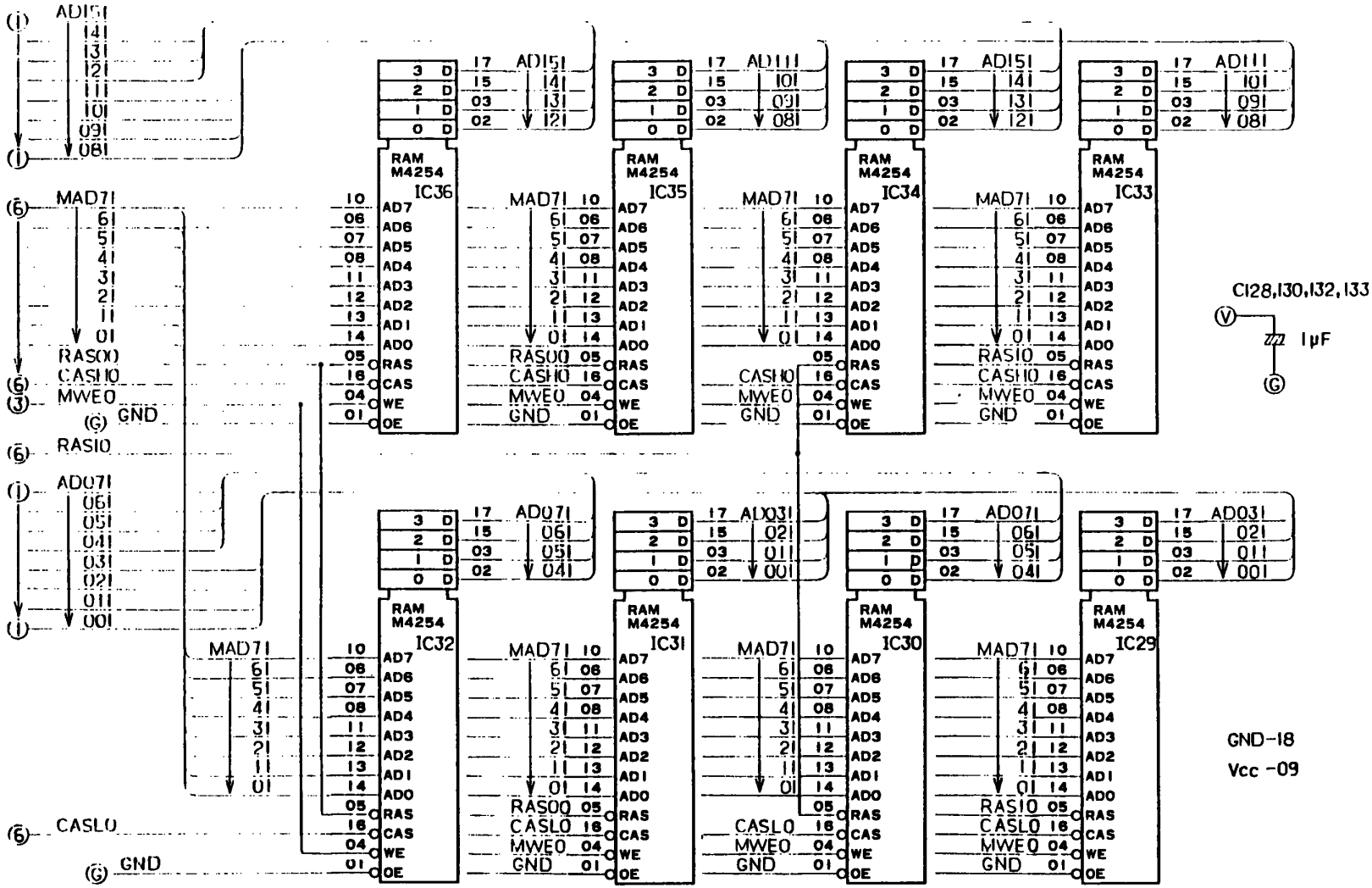
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE : PIC and TMR			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 5	DRAWING No.	PAGE No. 10	REV. MARK

TOSHIBA CORPORATION



REVISED BY	REVISED DATE	PRINTED BOARD	TITLE
			RAM DRIVER

CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No.	DRAWING No.	PAGE No.	REV MARK
			6		11	



REVISED BY	REVISED DATE	PRINTED BOARD	TITLE
			RAM ARRAY

CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No.	DRAWING No	PAGE No.	REV MARK
			7		12	

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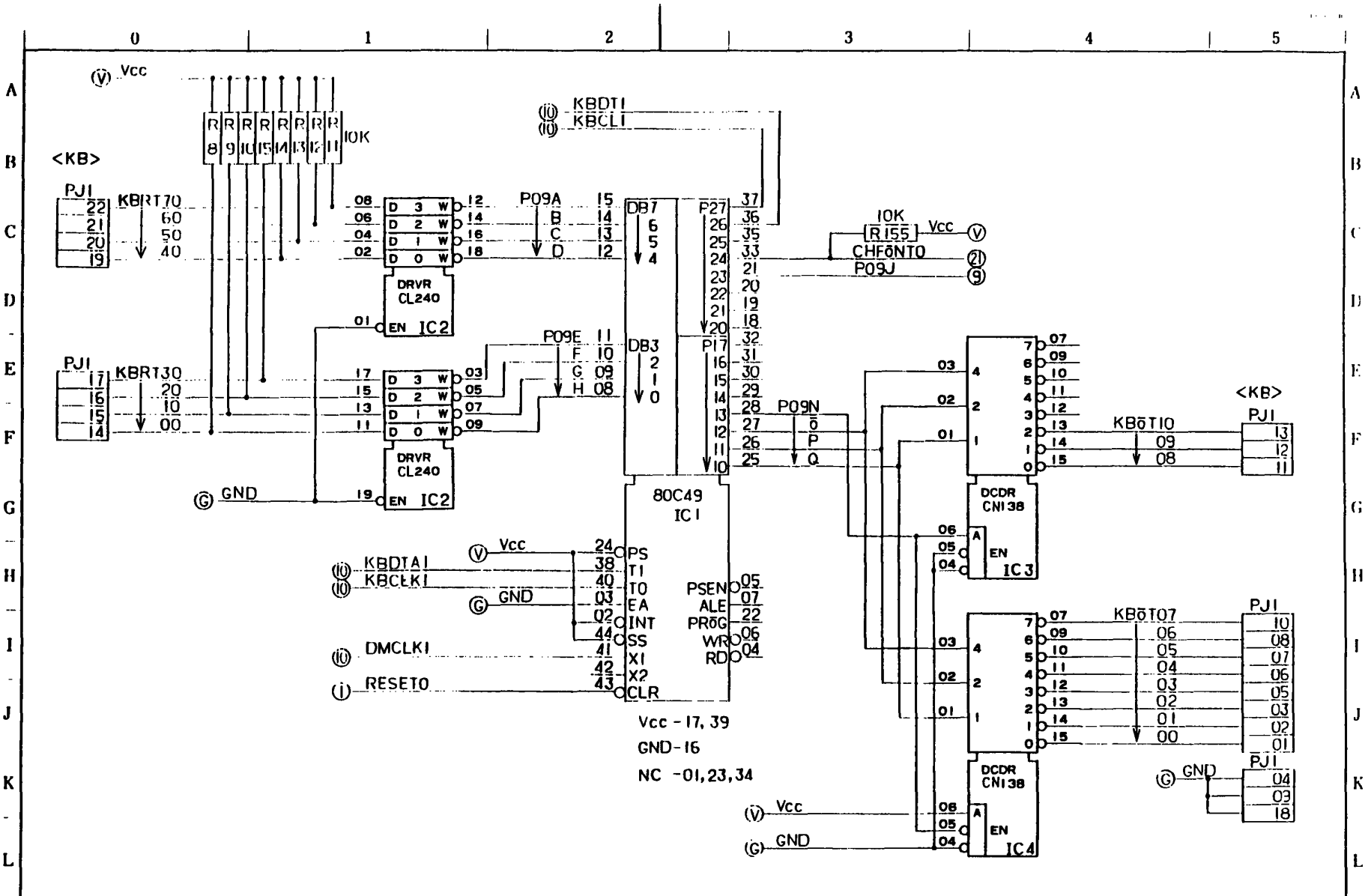

REVISED BY	REVISED DATE	PRINTED BOARD	TITLE: KEY BOARD INTERFACE			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No. 8	DRAWING No.	PAGE No. 13	REV MARK

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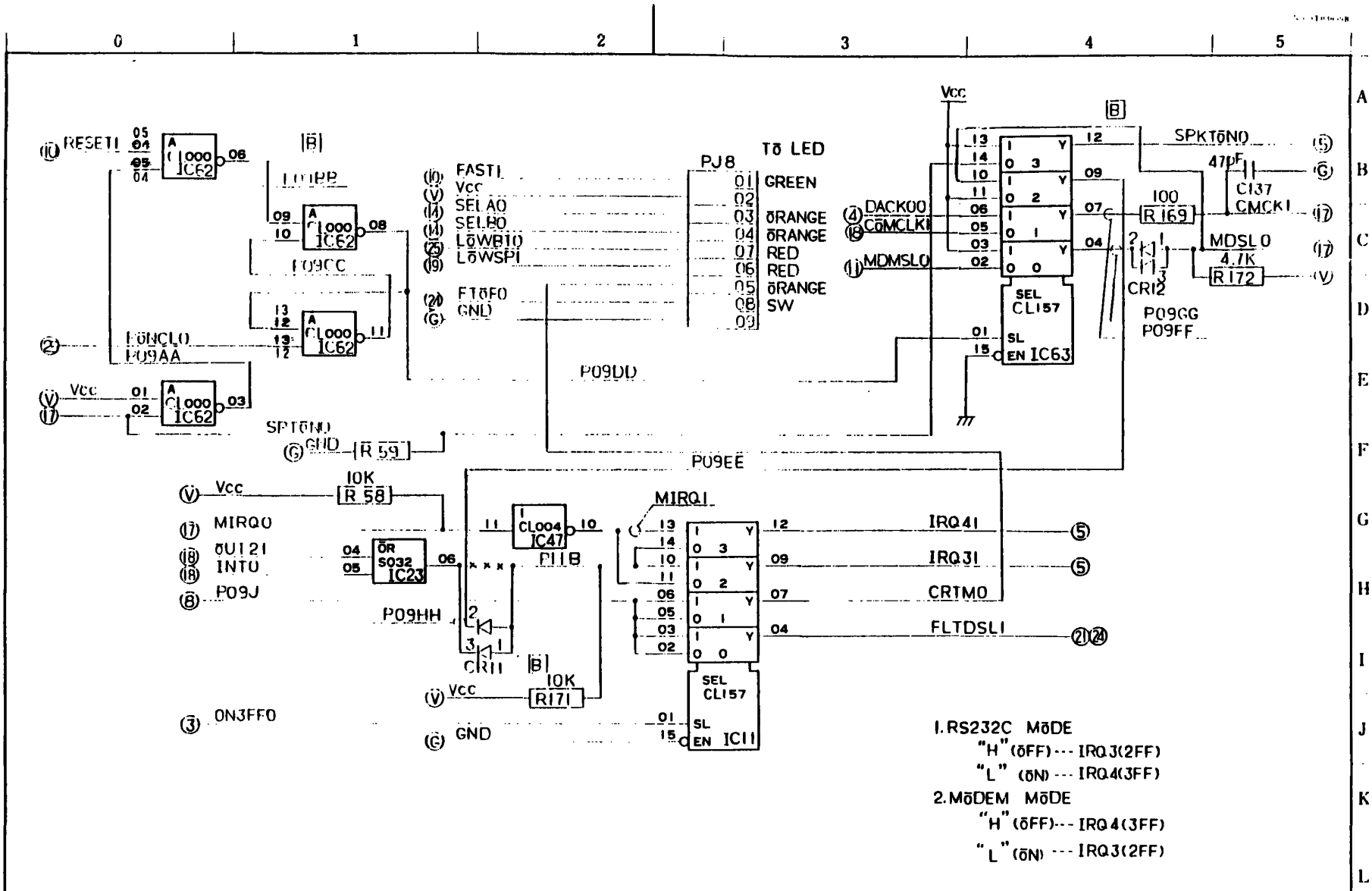

REVISED BY	REVISED DATE	PRINTED BOARD	TITLE: LED CONNECTER, RS232C SELECT				
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No. 9	DRAWING No.	PAGE No. 14	REV MARK	

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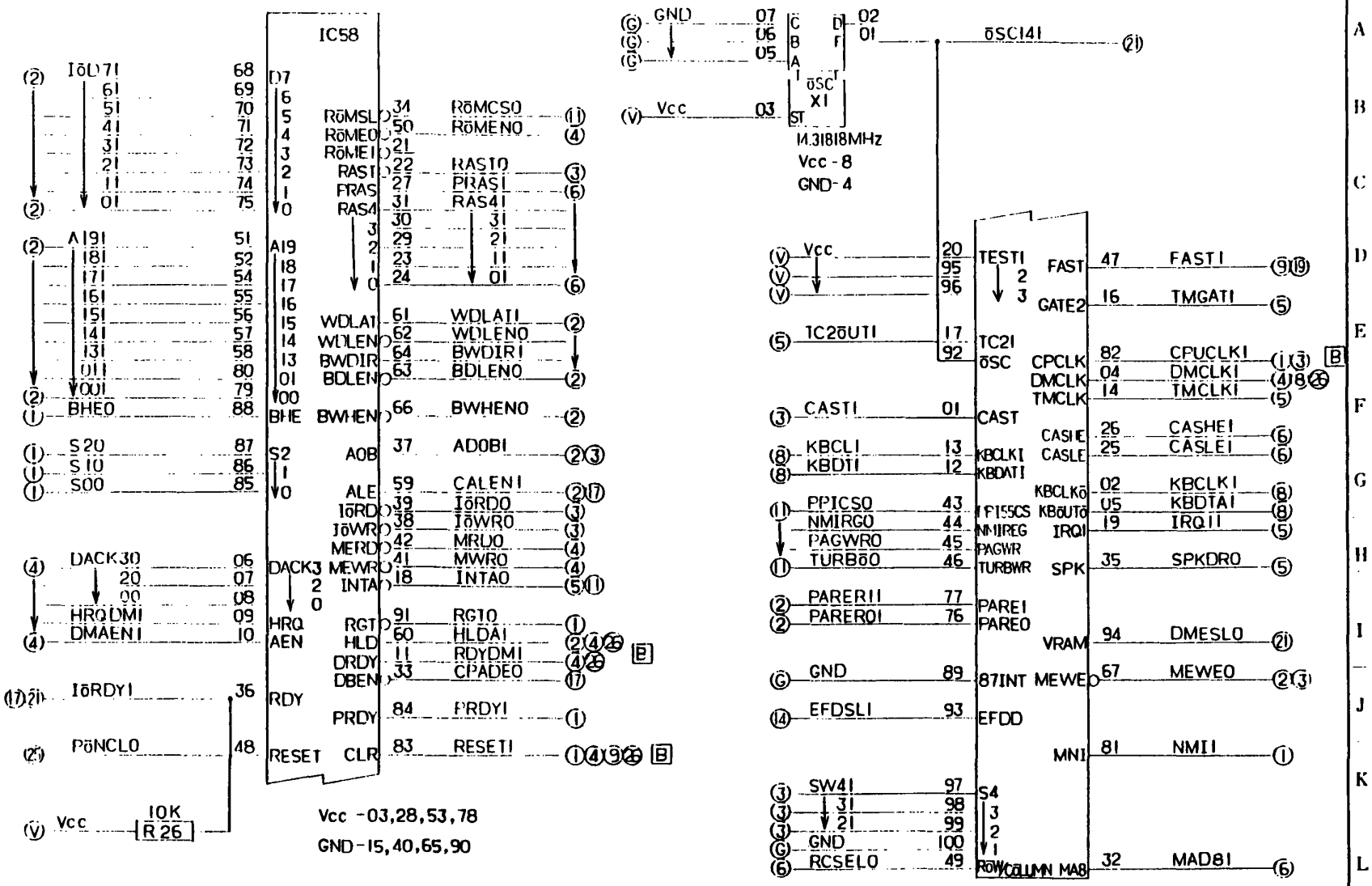

REVISED BY	REVISED DATE	PRINTED BOARD	TITLE: BUS CNT GA			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 10	DRAWING No.	PAGE No. 15	REV. MARK

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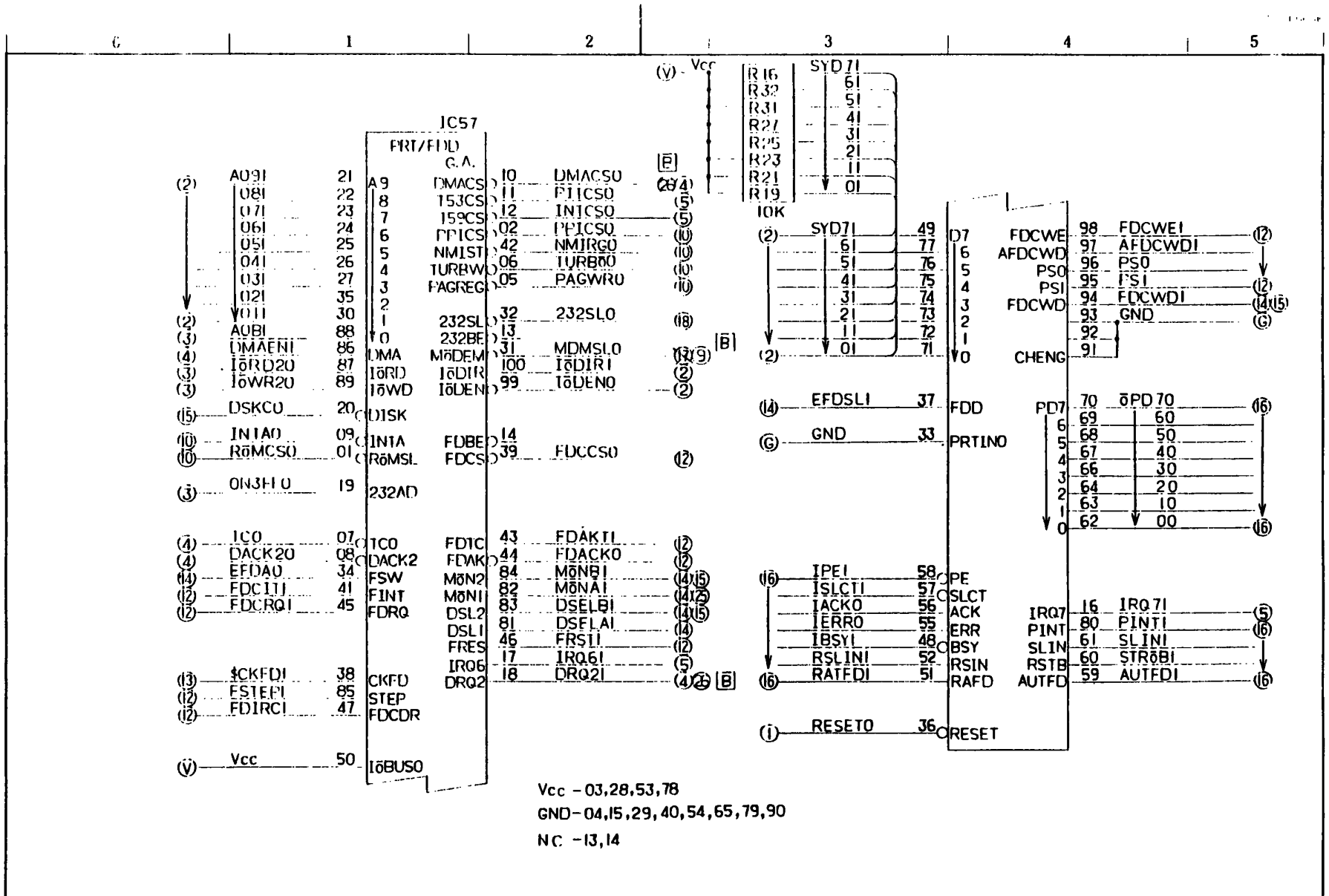

REVISED BY	REVISED DATE	PRINTED BOARD	TITLE: Iō DECōDER GA				
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 11	DRAWING No.	PAGE No. 16	REV. MARK	

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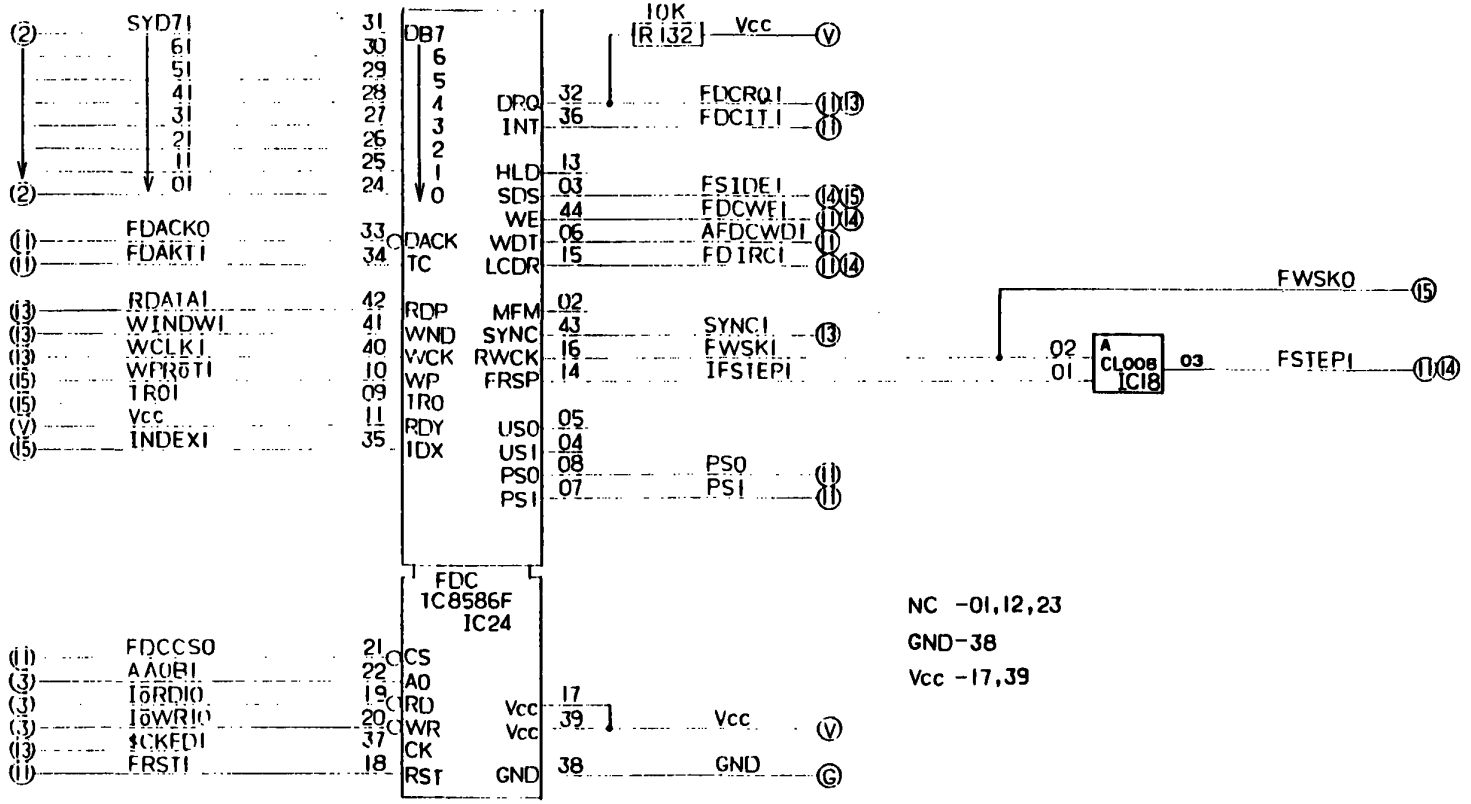
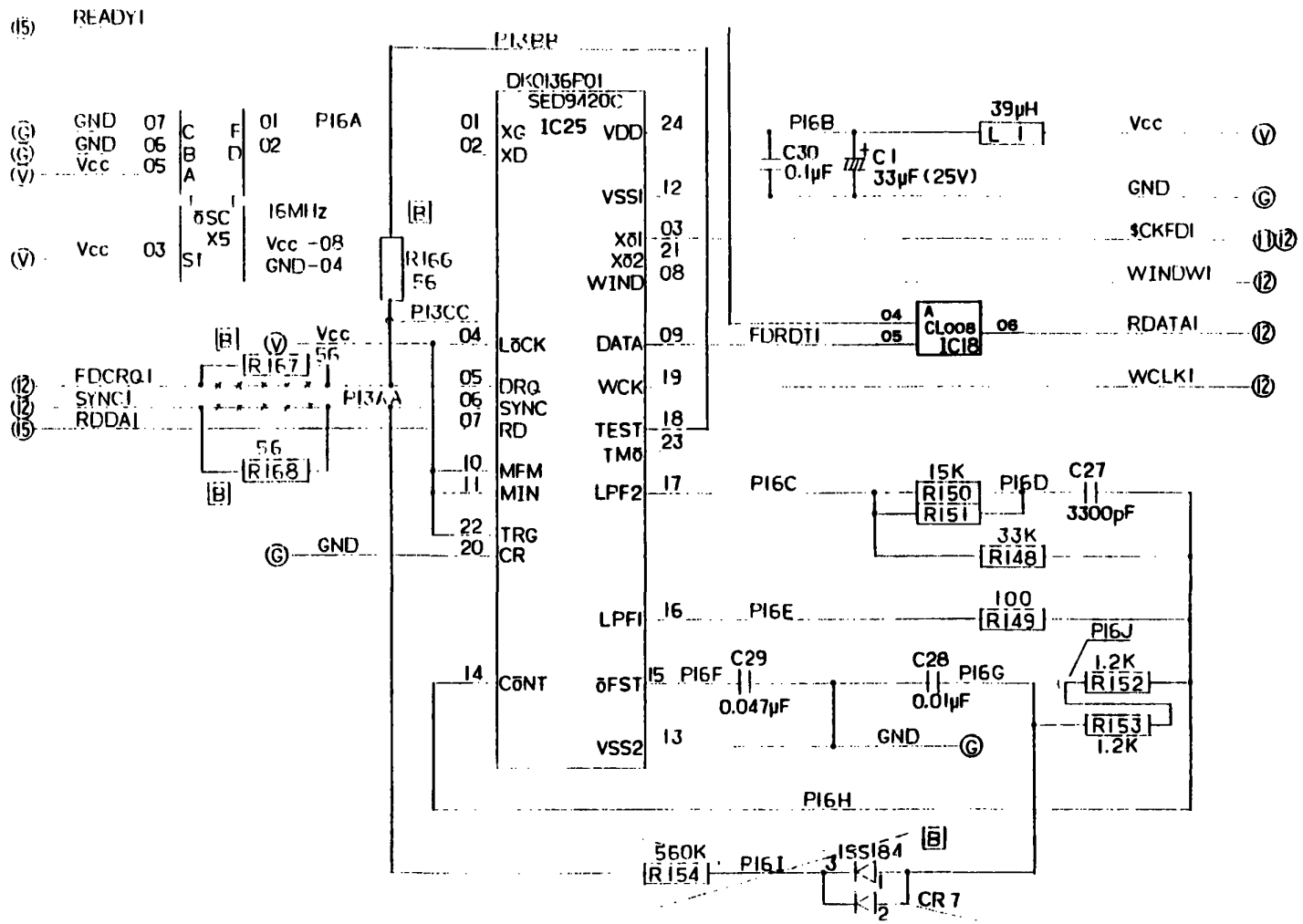


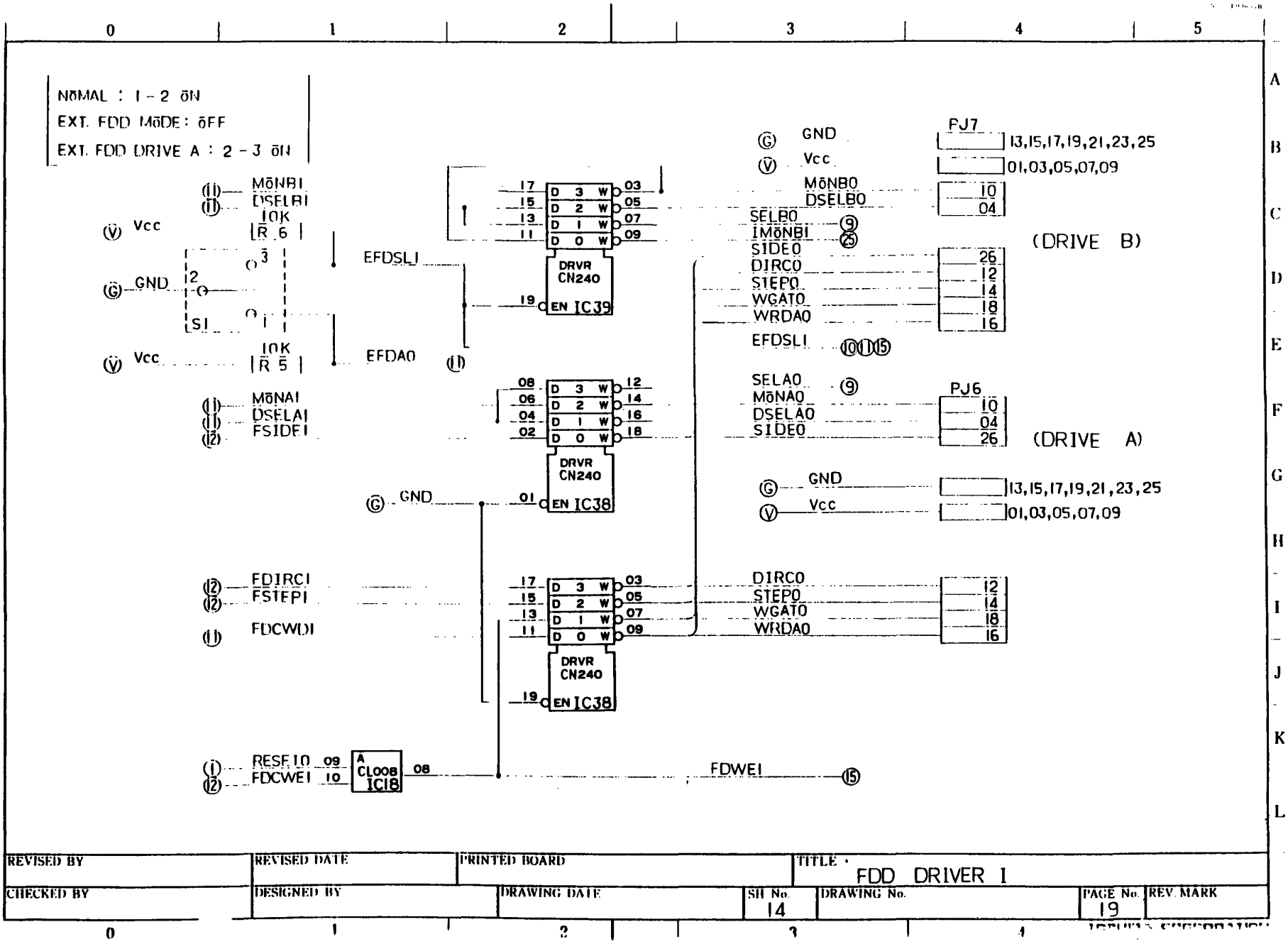
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE : FDC				
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No 12	DRAWING No.		PAGE No. 17	REV. MARK

TOSHIBA CORPORATION

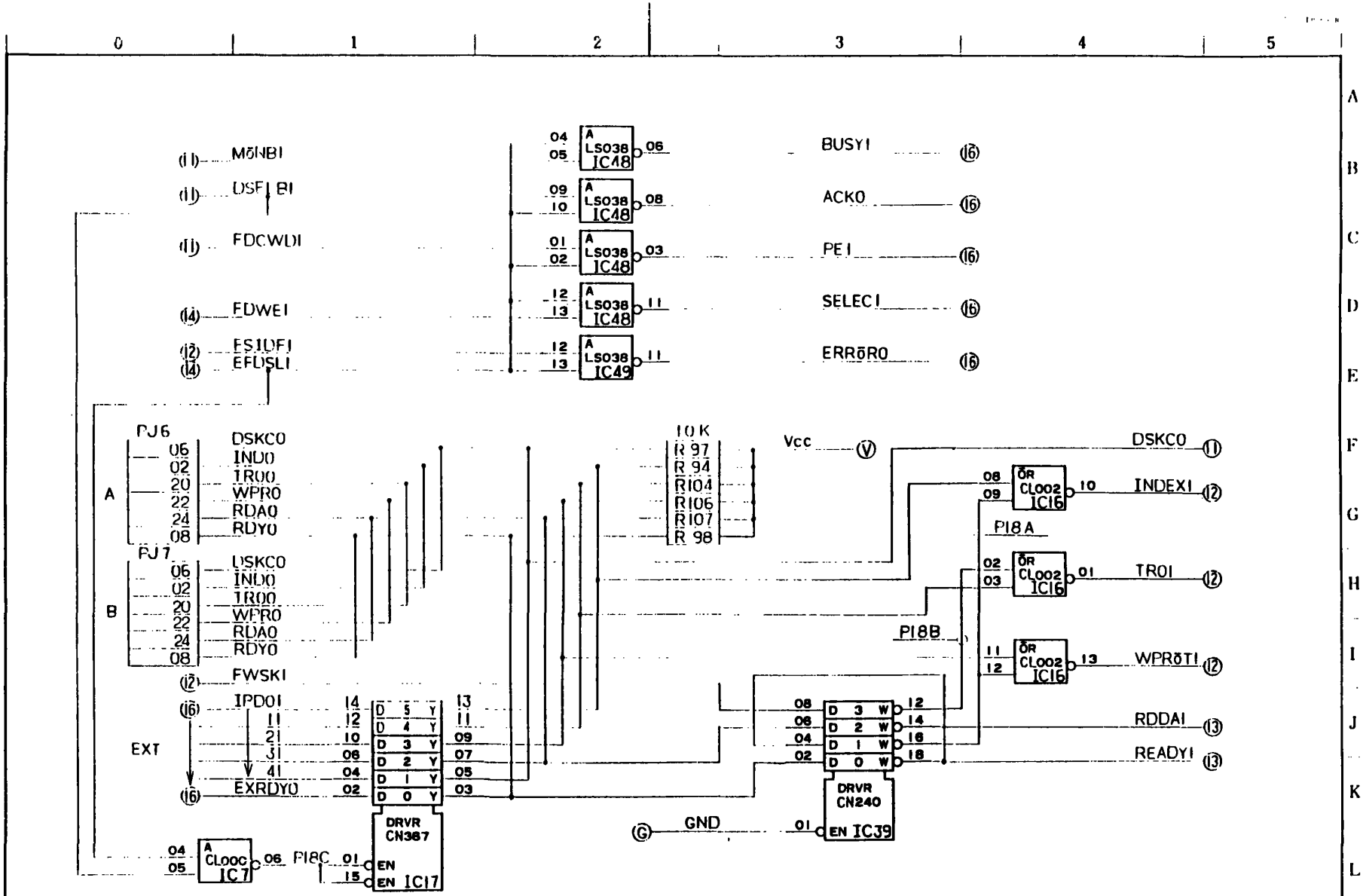


REVISED BY	REVISED DATE	PRINTED BOARD	TITLE : VFO			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No 13	DRAWING No	PAGE No. 18	REV MARK

TOSHIBA CORPORATION

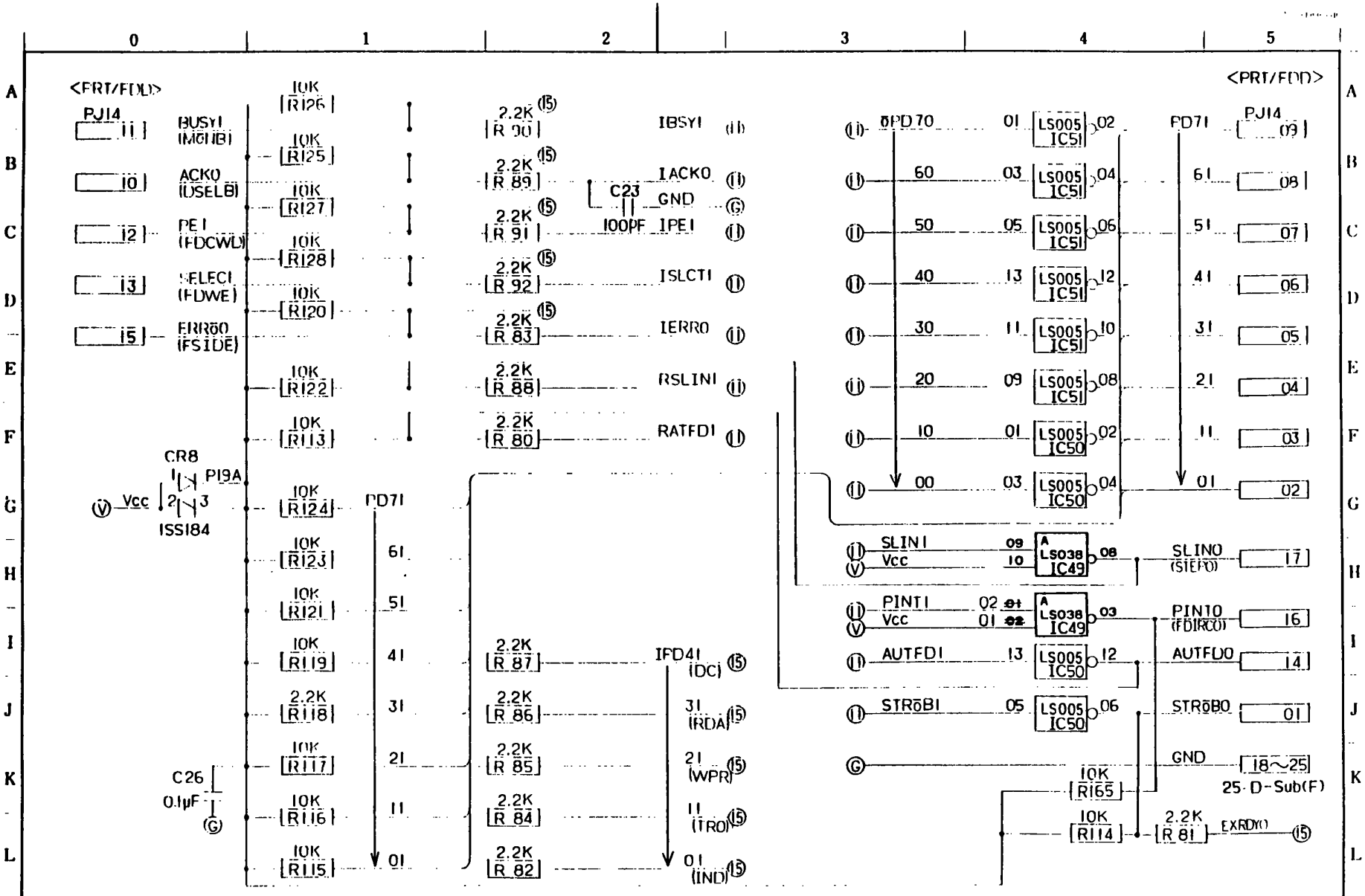


REVISED BY	REVISED DATE	PRINTED BOARD	TITLE : FDD DRIVER 1			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No. 14	DRAWING No.	PAGE No. 19	REV. MARK



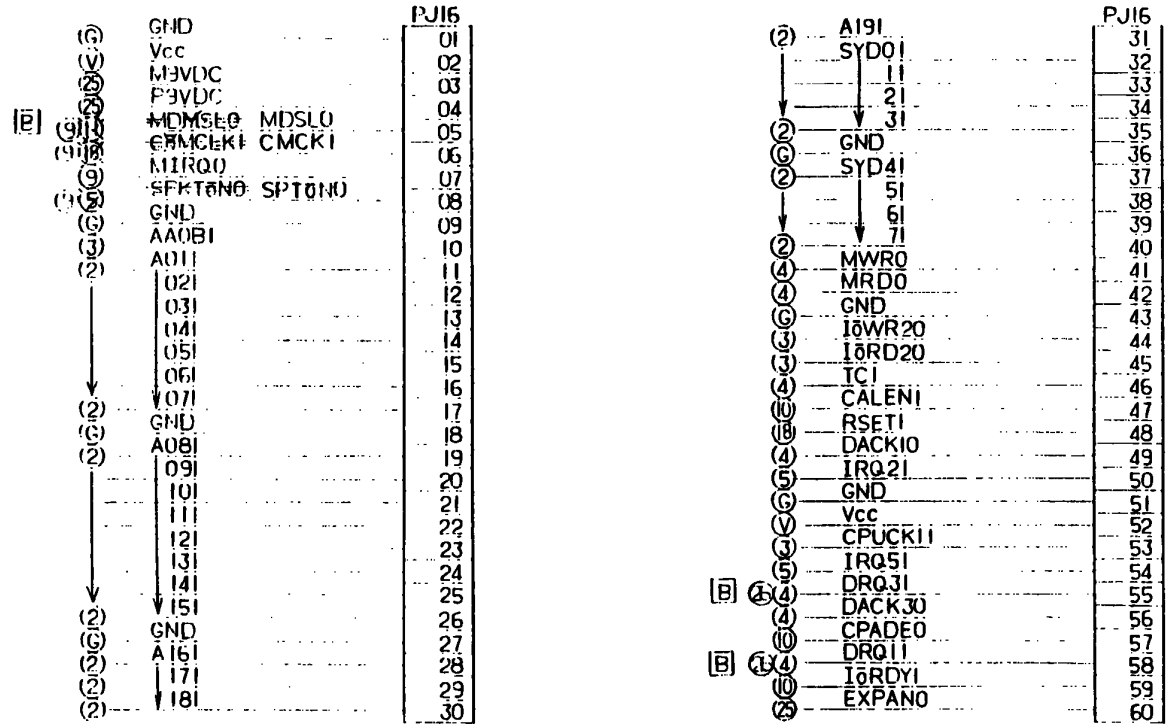
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE: FDD DRIVER II				
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 15	DRAWING No.	PAGE No. 20	REV MARK	

TOSHIBA CORPORATION



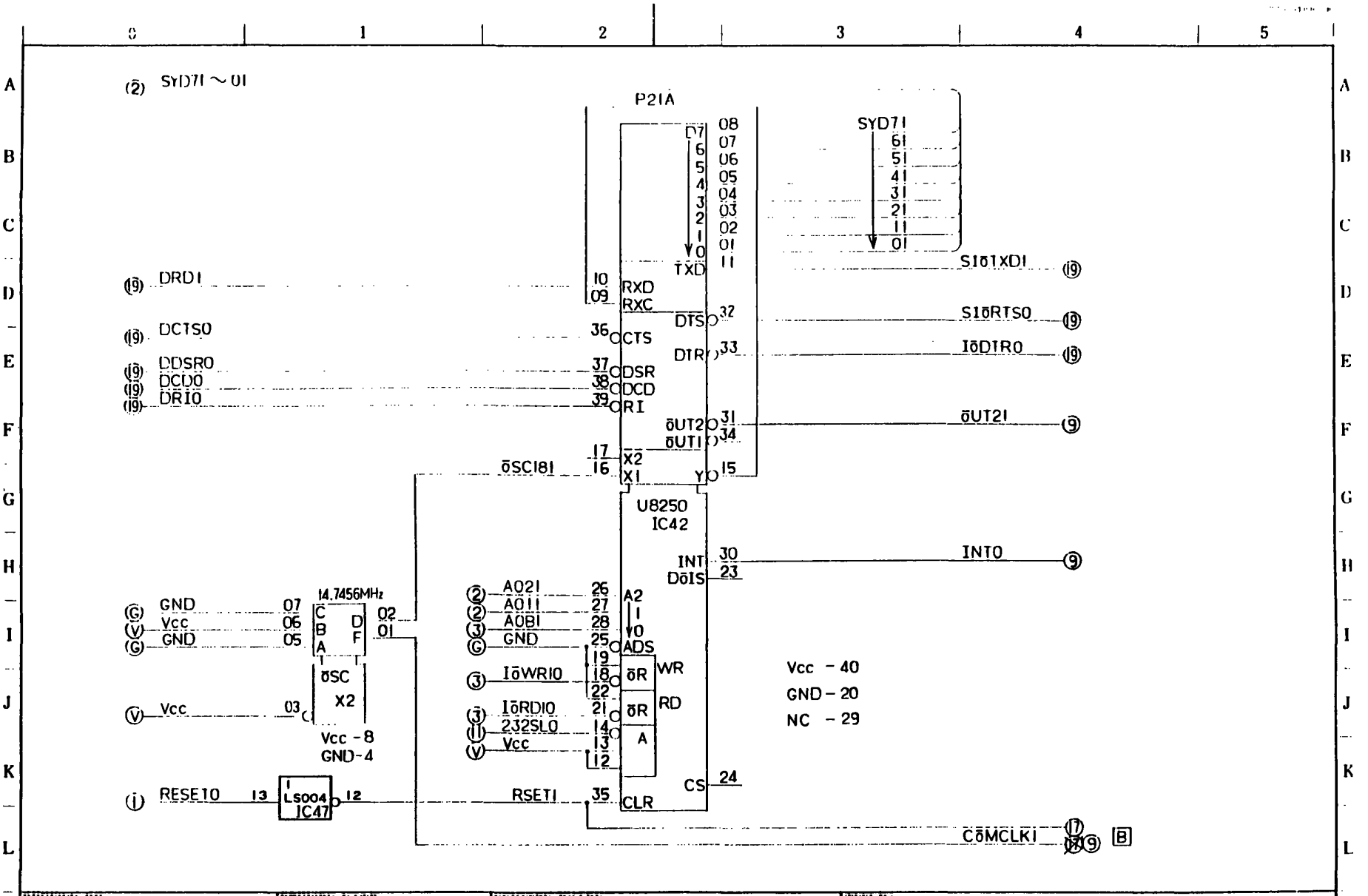
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE : PRT/FDD INTERFACE			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No. 16	DRAWING No	PAGE No 21	REV MARK

TOSHIBA CORPORATION



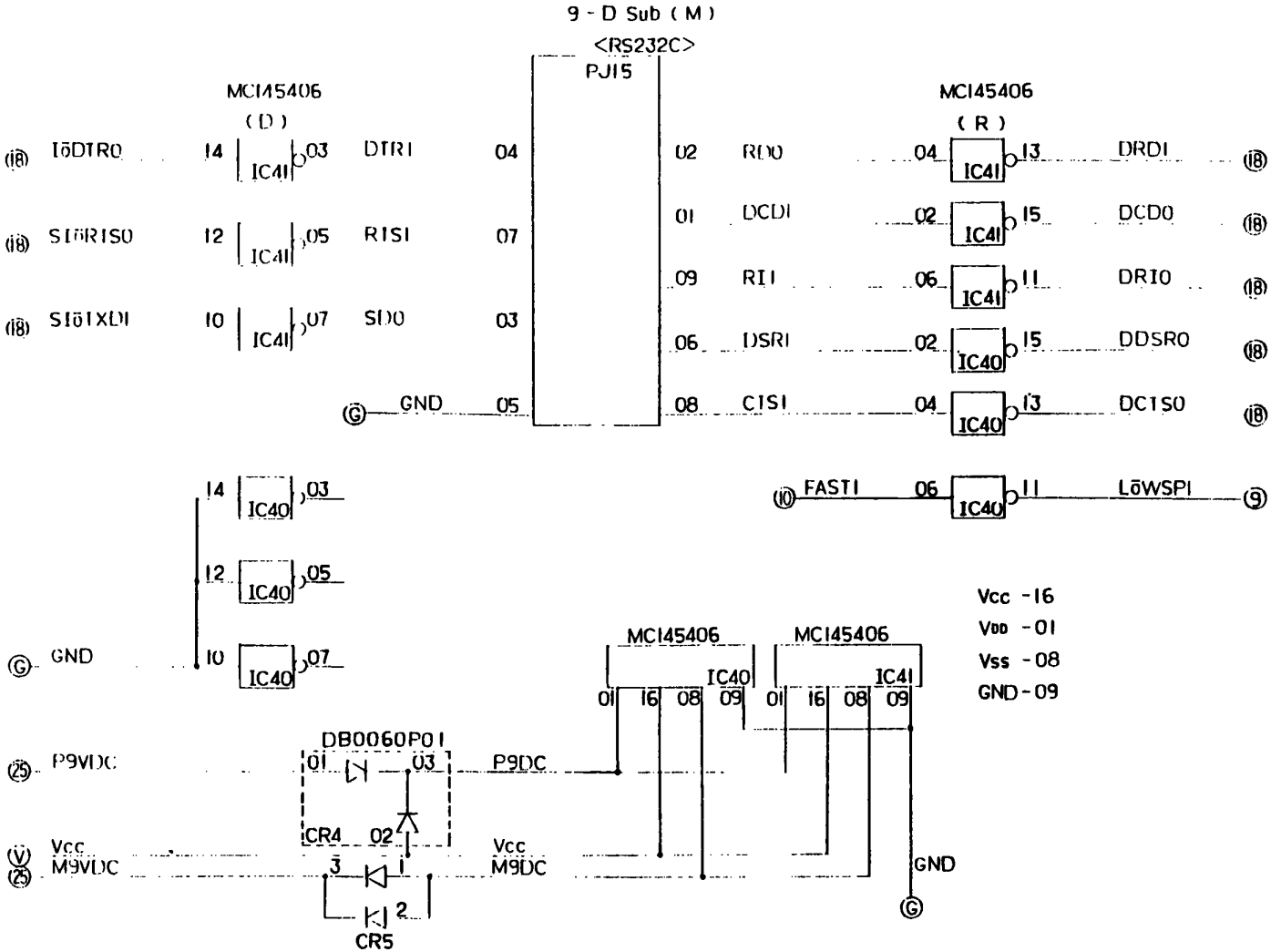
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE : EXPANSION BUS			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No 17	DRAWING No	PAGE No. 22	REV MARK

TOSHIBA CORPORATION



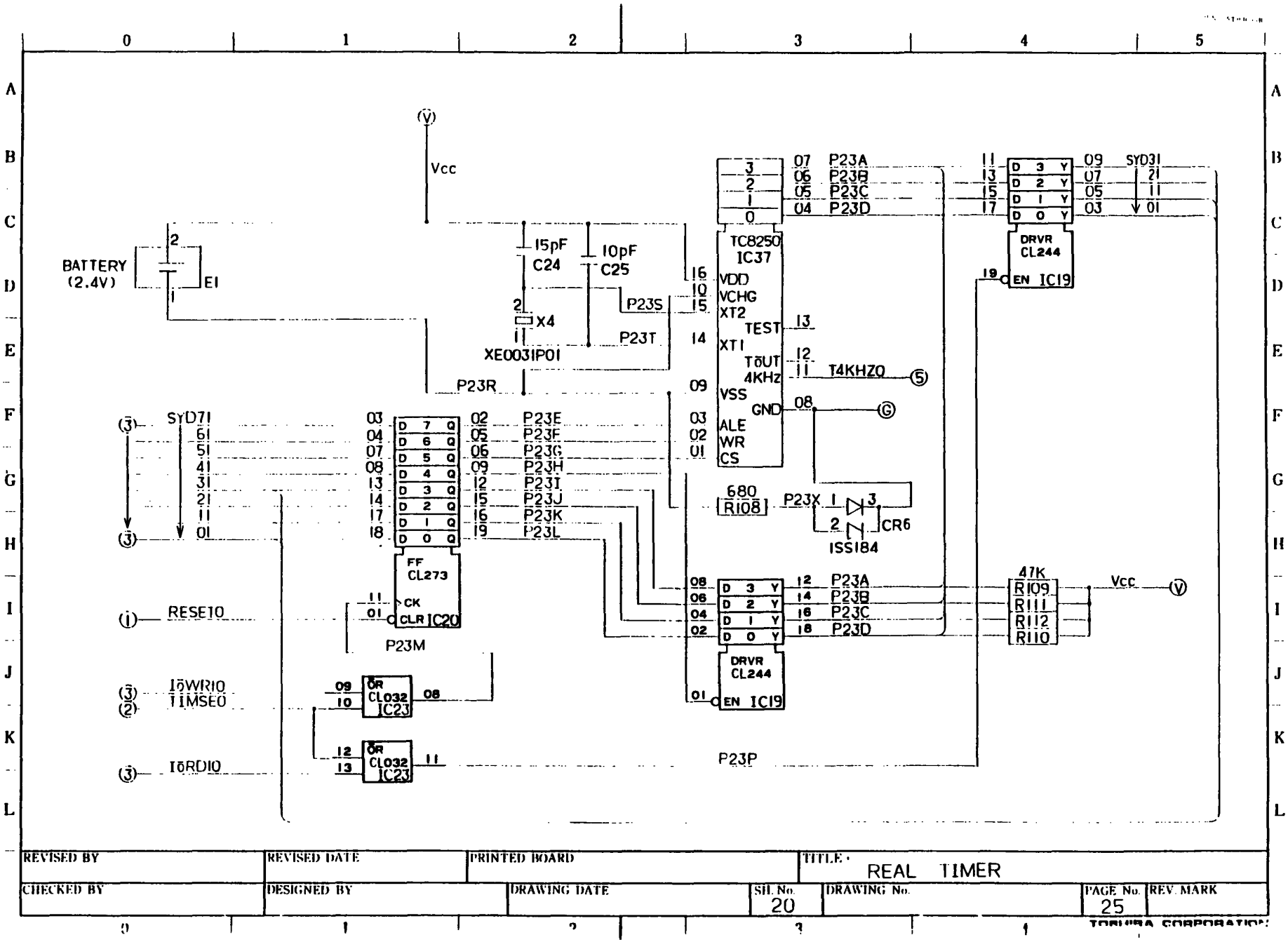
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE: RS232C CōNTRōLLER			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No. 18	DRAWING No.	PAGE No. 23	REV. MARK

TOSHIBA CORPORATION



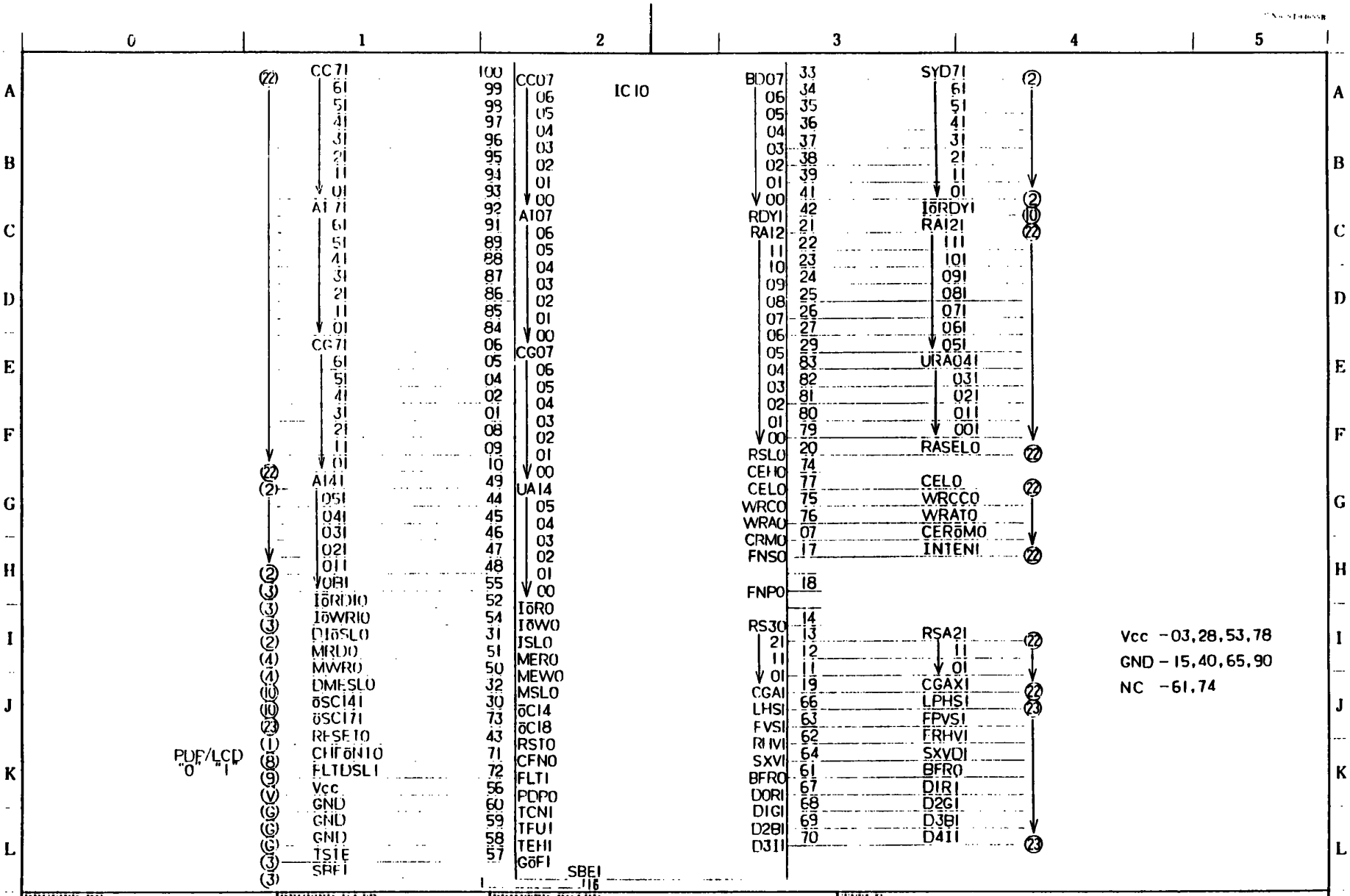
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE : DRIVER/RECEIVER(RS232C)			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 19	DRAWING No.	PAGE No. 24	REV. MARK

TOSHIBA CORPORATION



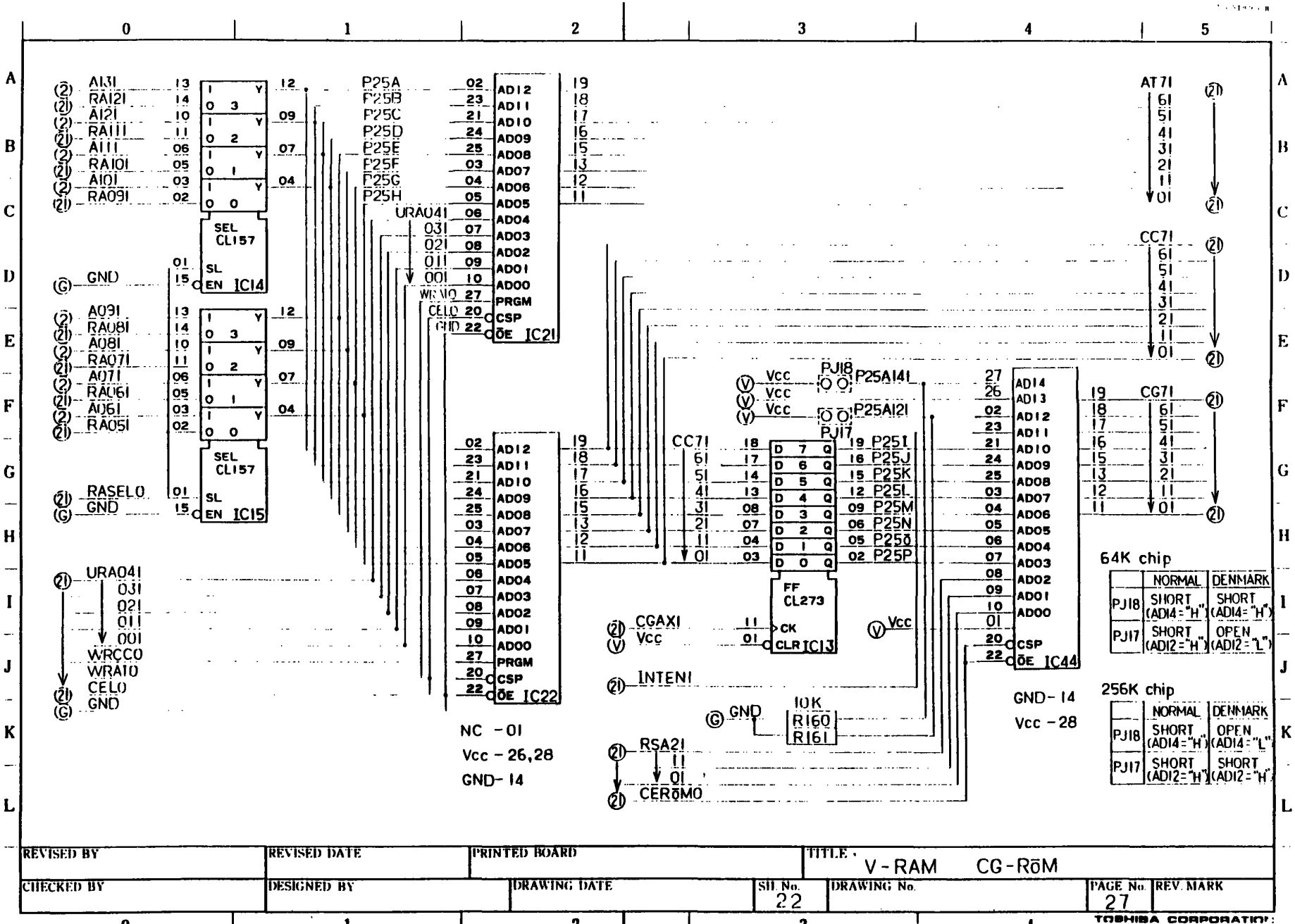
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE: REAL TIMER			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 20	DRAWING No.	PAGE No. 25	REV. MARK

TOSHIBA CORPORATION



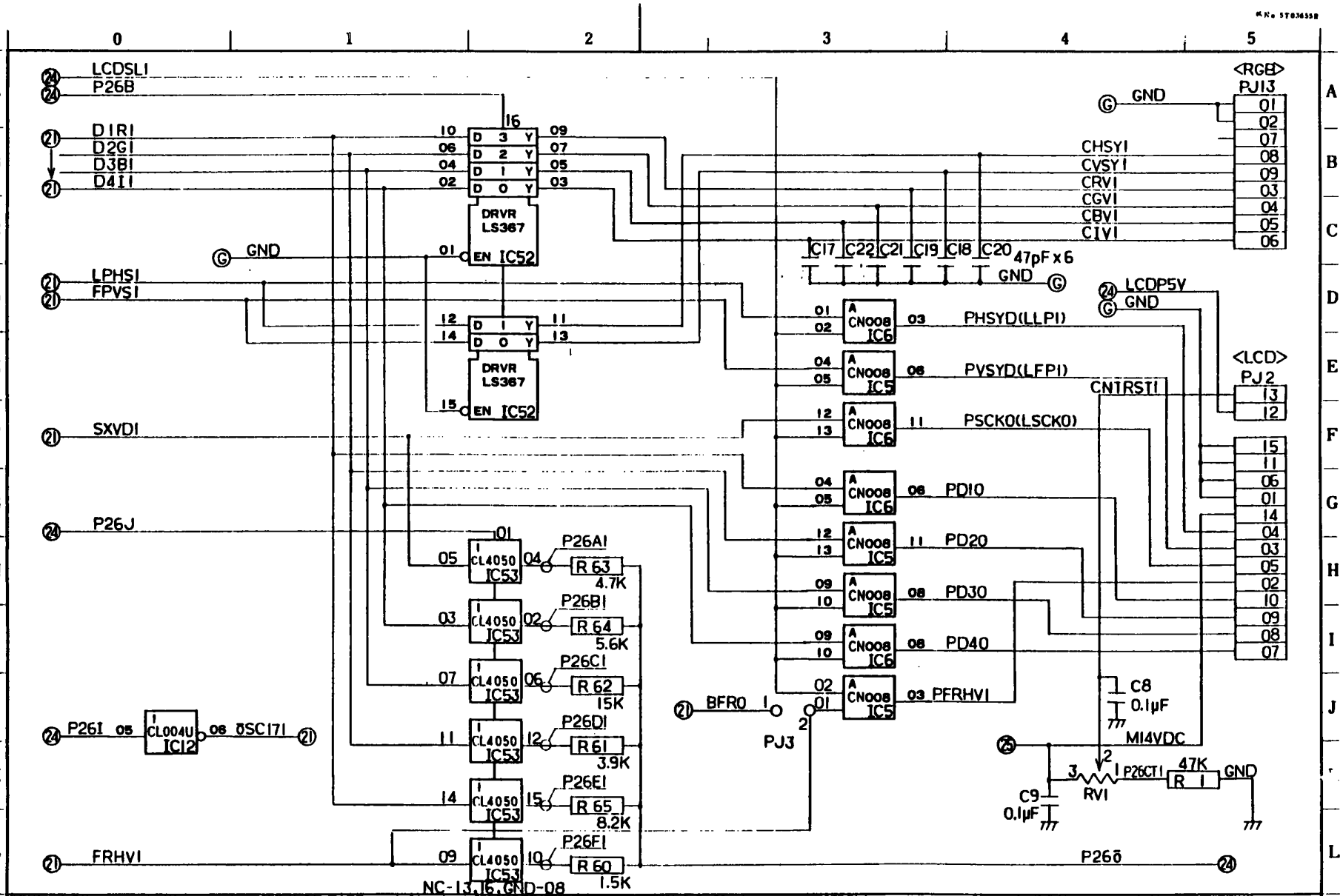
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE : DISPLAY GA			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 21	DRAWING No	PAGE No. 26	REV. MARK

TOSHIBA CORPORATION



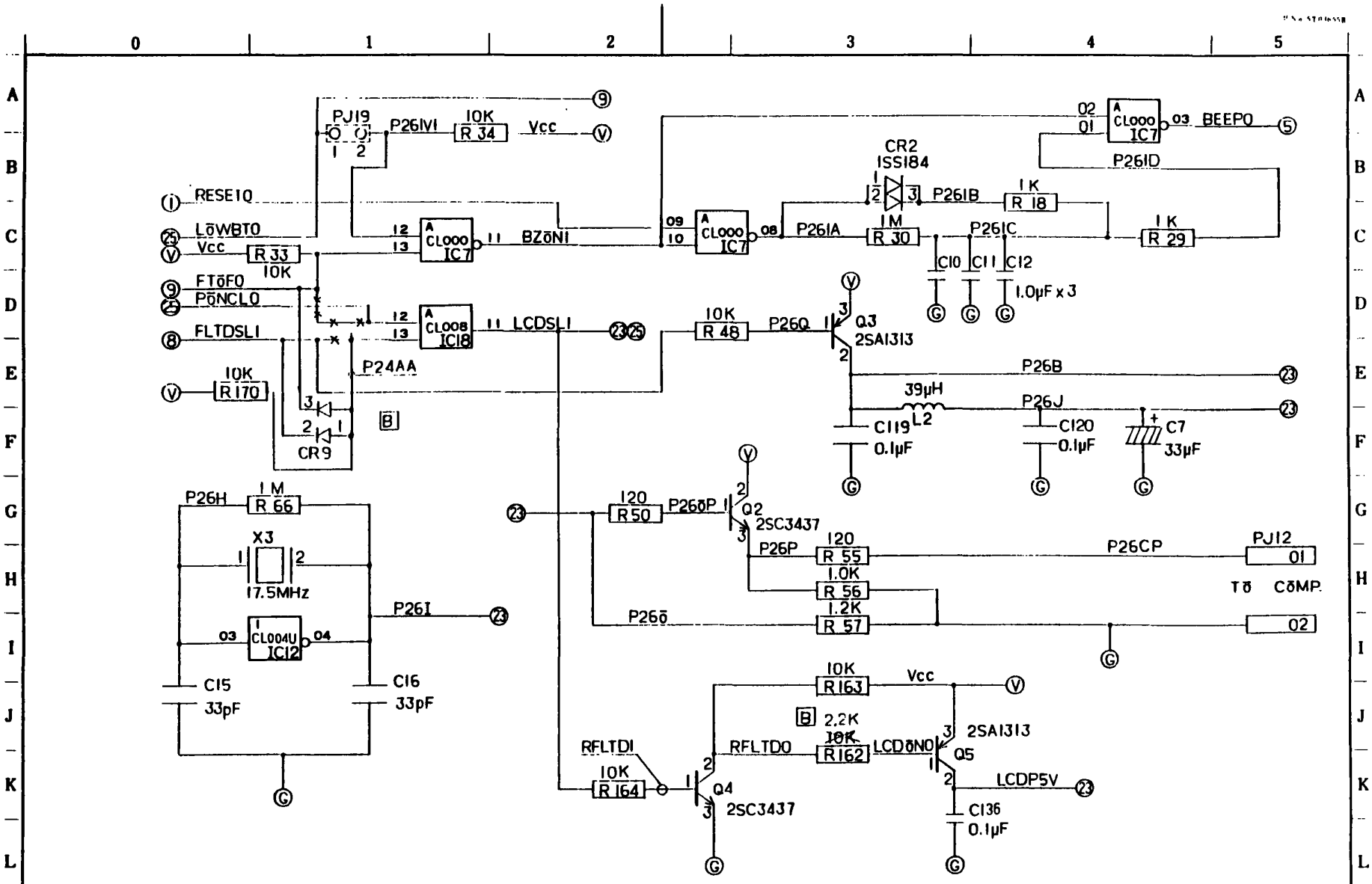
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE: V-RAM CG-RŌM			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 22	DRAWING No.	PAGE No. 27	REV. MARK

TOSHIBA CORPORATION



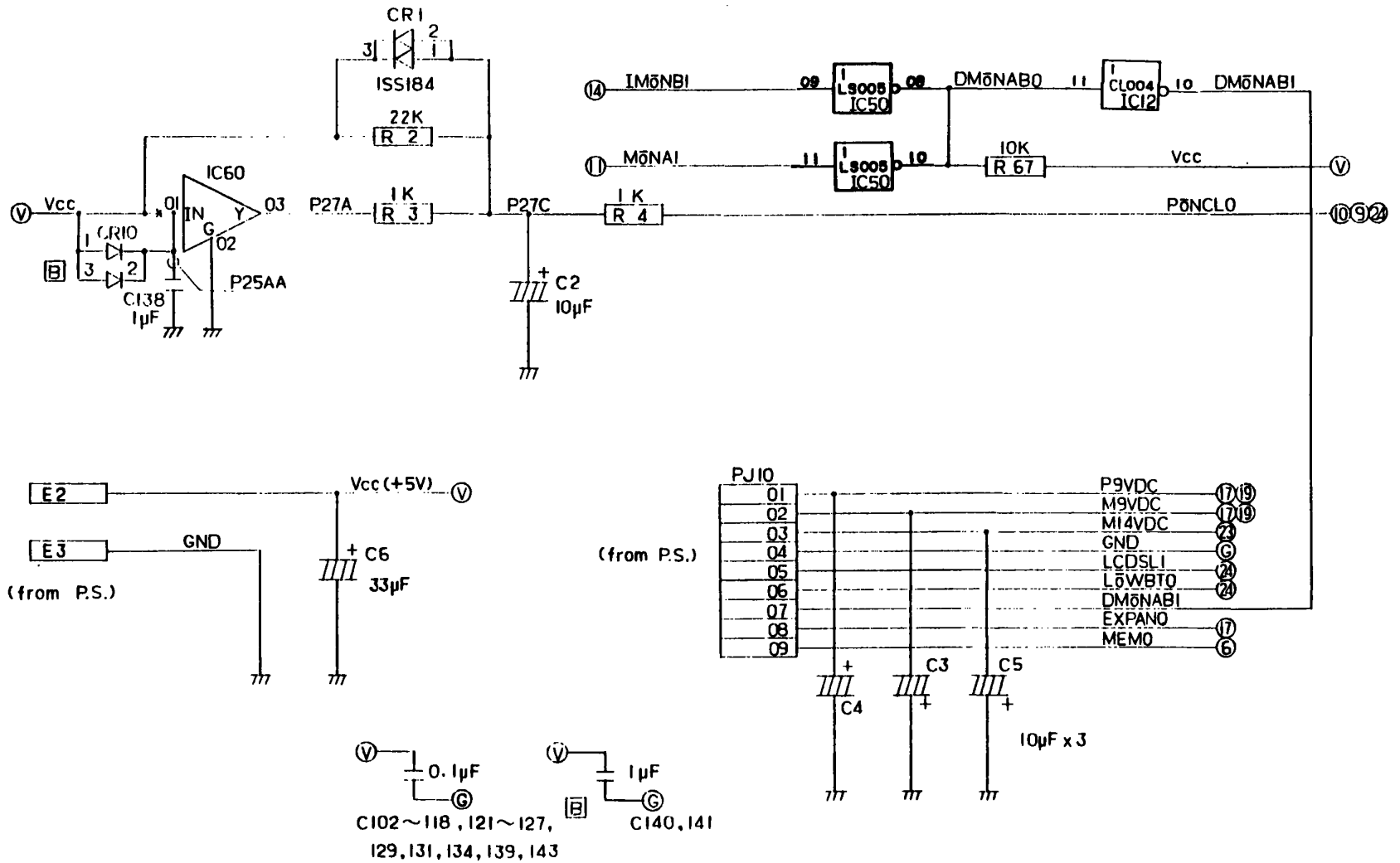
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE				
			DISPLAY DRIVER I				
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 23	DRAWING No.	PAGE No. 28	REV. MARK	

TOSHIBA CORPORATION



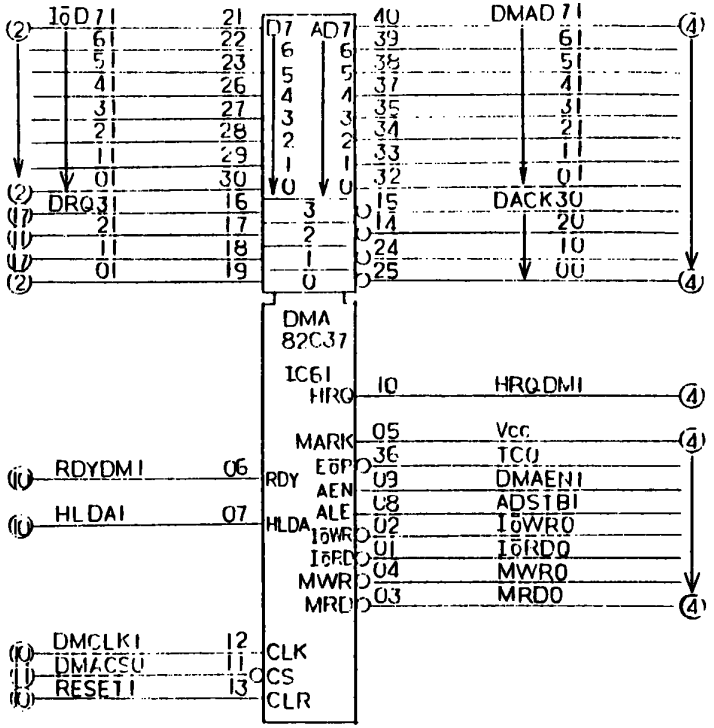
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE. DISPLAY DRIVER II			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 24	DRAWING No.	PAGE No. 29	REV. MARK

TOSHIBA CORPORATION



REVISED BY	REVISED DATE	PRINTED BOARD	TITLE: PS			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No. 25/5	DRAWING No.	PAGE No. 30/5	REV. MARK

TOSHIBA CORPORATION



REVISED BY	REVISED DATE	PRINTED BOARD	TITLE: DMA			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 26/F	DRAWING No.	PAGE No 31/F	REV. MARK B

TOSHIBA CORPORATION

TOSHIBA

FPLPSI

T1100PLUS

POWER SUPPLY BOARD

34M741476G01

変更回数 REV. MARK	記事 CONTENTS	承認 APPROVED BY	担当 REVISED BY	保管 REGISTERED
A0	発行 ISSUE		A.SHINMI 1986・1・20	
B0	R8削除, R14,30,50,C4 定数変更 (Delete R8 Change R14,30,50,C4)		A.SHINMI 1986・9・25	
C	R42, R50 定数変更 (Change R42, R50)	T.Yamazaki June・3'86	S. Morioka 1986・10・30	

PAGE	題目 TITLE		PAGE	題目 TITLE	
1	COVER SHEET		26		
2	CHARGE CIRCUIT	B	27		
3	REGULATOR	B	28		
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25			50		

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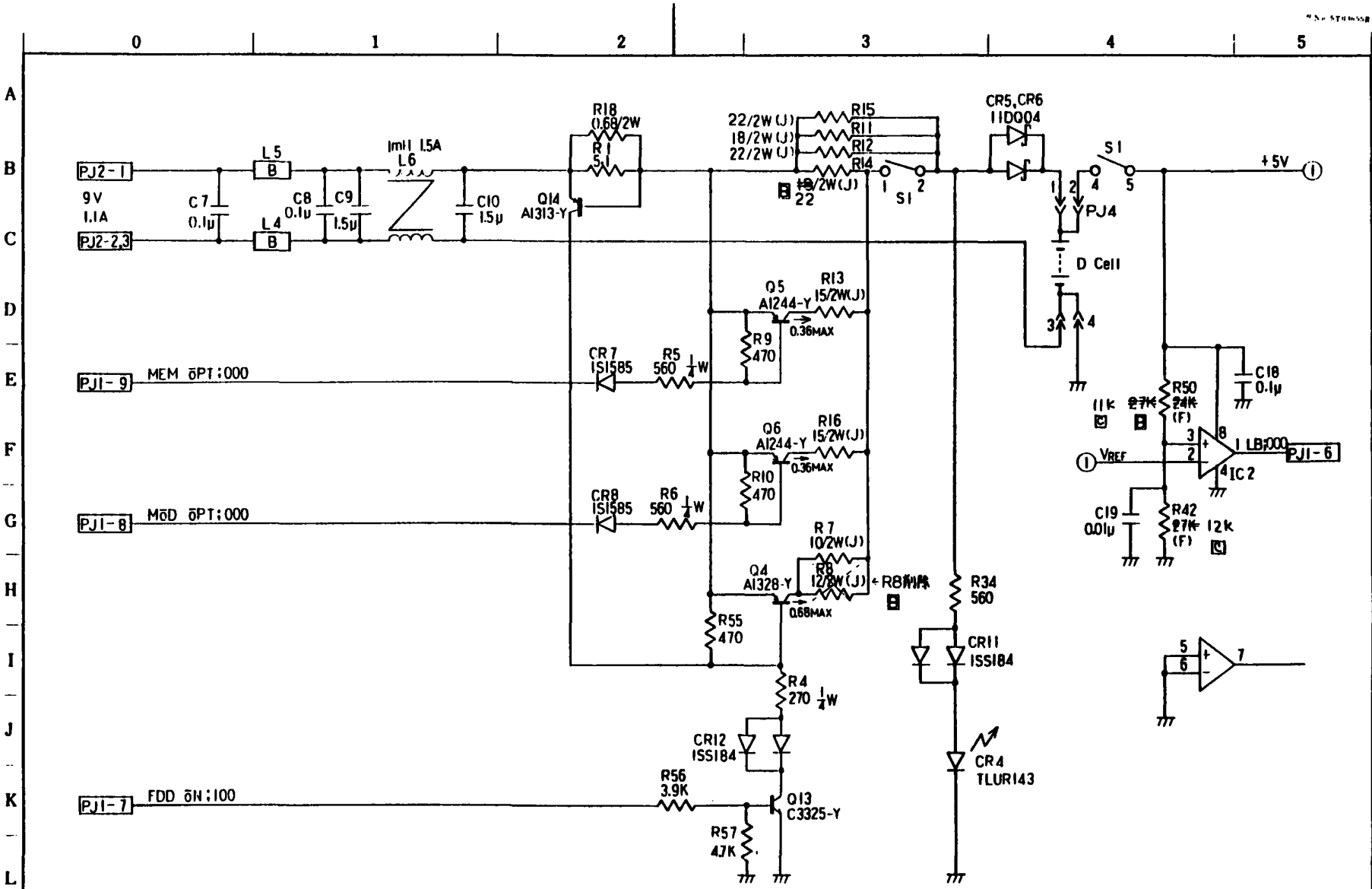
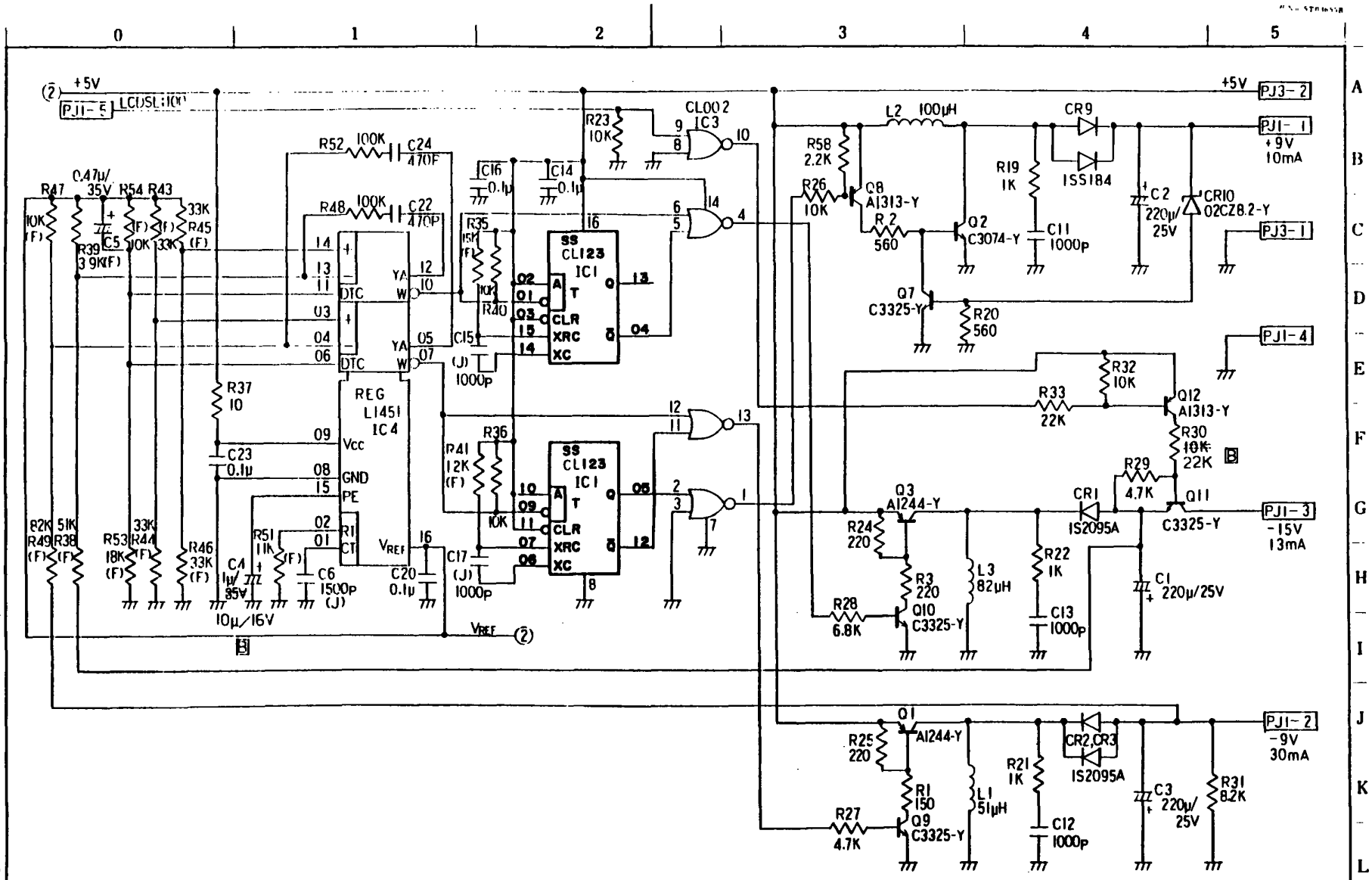
ML (有・無)

承認 APPROVED BY	検図 CHECKED BY	設計 DESIGNED BY	製図 DRAWN BY	図面番号 DRAWING NO.
T.Yamazaki June・3'86		S. Morioka 1986・1・20	A.SHINMI 1986・1・20	72M14021B
保管 REGISTERED				TOTAL 3 CONT. ON 2 PAGE NO. 1



REVISED BY	REVISED DATE	PRINTED BOARD	TITLE				
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No.	DRAWING No.		PAGE No. 2	REV. MARK C

TOSHIBA CORPORATION



REVISED BY	REVISED DATE	PRINTED BOARD	TITLE				
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No.	DRAWING No.		PAGE No. 3F	REV. MARK B

TOSHIBA CORPORATION

TOSHIBA

FPLED1·2

T1100PLUS

LED BOARD

FPLED1 - 34M741486G01

FPLED2 - 34M741576G01

変更回数 REV. MARK	記事 CONTENTS	承認 APPROVED BY	担当 REVISED BY	保管 REGISTERED
A0	発行 ISSUE	F.Yamazaki June·3·'86	A.SHINMI 1986·4·28	· ·
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11		36	
12		37	
13		38	
14		39	
15		40	
16		41	
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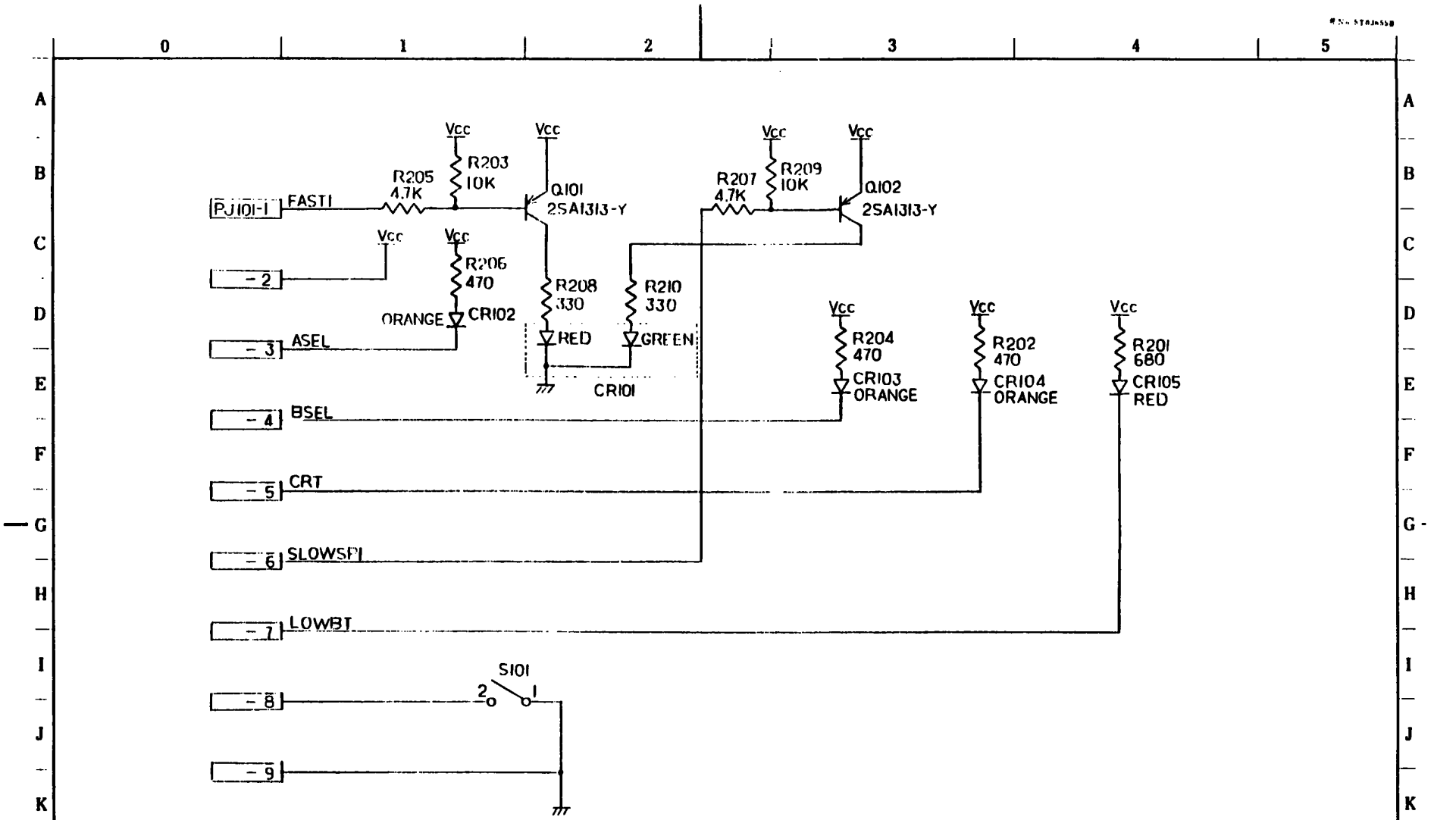
ML (有・無)

承認 APPROVED BY	検図 CHECKED BY	設計 DESIGNED BY	製図 DRAWN BY	図面番号 DRAWING NO
F.Yamazaki June·3·'86	· ·	A.SHINMI 1986·9·28	A.SHINMI 1986·4·28	72M140864
保管 REGISTERED · ·				TOTAL 2 CONT. ON 2 PAGE NO. 1



REVISED BY	REVISED DATE	PRINTED BOARD	TITLE			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No.	DRAWING No.	PAGE No. 2F	REV. MARK

TOSHIBA CORPORATION

BNo. ST03655-1B

展開接続図 SCHEMATIC DIAGRAMS

T2100

F12MD2

MODEM BOARD

34P710881G01

変更回数 REV.MARK	記事 CONTENTS	承認 APPROVED BY	担当 REVISED BY	保管 REGISTERED
A	ISSUE	J.Makino '86·4·16	Y.Miyama '86·4·2	S.Nakade '86·5·9
B	変更 7, 9頁	J.Makino '86·6·4	K.Koji '86·6·4	..
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承認 APPROVED BY	検図 CHECKED BY	設計 DESIGNED BY	図面番号 DRAWING NO.	変更記号 REV.MARK
J.Makino '86·4·16	K.Koji 86·4·1	Y.Miyama '86·4·2	34M900069	B

品名記号 CODE

TOTAL 12 CONT. ON 2 PAGE NO. 1

PJ 4 SYSTEM INTERFACE

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	NC			02	VCC		8
03	M9VDC	O	1	01	NC		
05	MDMSLO	I		06	COMCLK1	I	2
07	MIRQO;000	O	7	08	MDSPk;000	O	6
09	DGND		8	10	AA0B1	I	1
11	A011	I	1	12	A021	I	1
13	NC			11	NC		
15	NC			16	NC		
17	NC			18	DGND		8
19	NC			20	NC		
21	NC			22	NC		
23	NC			21	NC		
25	NC			26	NC		
27	DGND		8	28	NC		
29	NC			30	NC		
31	NC			32	SYD01	O	1
33	SYD11	O	1	31	SYD21	O	1
35	SYD31	O	1	36	DGND		8
37	SYD41	O	1	38	SYD51	O	1
39	SYD61	O	1	10	SYD71	O	1
41	NC			12	NC		
43	DGND		8	11	IOWR20	I	1
15	IORD20	I	1	16	NC		
17	NC			18	RSET1	I	1
19	NC			50	NC		
51	DGND		8	52	NC		
53	NC			54	NC		
55	NC			56	NC		
57	NC			58	NC		
59	NC			60	PWRON;000	O	7

PJ 1 TELEPHONE 1

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	NC			02	A1	I/O	4
03	TIP1	I/O	4	01	RING1	I/O	4
05	A11	I/O	4	06	NC		
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			
21				22			
23				24			
25				26			
27				28			
29				30			
31				32			
33				34			
35				36			
37				38			
39				10			
41				42			
13				44			

PJ 2 TELEPHONE 2

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	NC			02	A2	I/O	4
03	TIP2	I/O	4	01	RING2	I/O	4
05	A12	I/O	4	06	NC		
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			
21				22			
23				24			
25				26			

PJ 5 DTR CONTROL

PIN	SIG. NAME	I/O	SH	PIO	SIG. NAME	I/O	SH
01	SIODTR;000	I	1	02	DTR	O	1
03	NC		2	01			
05				06			
07				08			

PJ 6 CD CONTROL

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	PD4	O	2	02	SIODCD;000	I	2
03	NC		2	04			
05				06			
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			

REVISED BY	REVISED DATE	PRINTED BOARD	TITLE	CONNECTOR PIN SIGNAL MAP 1	
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No.	DRAWING No.	PAGE No. 2 / REV. MARK A

TOSHIBA CORPORATION

PJ7 LINE CONTROL

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	LINE 1	I/O	4	02	LINE 2	I/O	4
03	NC		4	01			
05				06			
07				08			
09				10			
11				12			
13				11			
15				16			
17				18			
19				20			
21				22			
23				21			
25				26			
27				28			
29				30			
31				32			
33				31			
35				36			
37				38			
39				10			
11				12			
13				11			
15				16			
17				18			
19				50			

PJ

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01				02			
03				01			
05				06			
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			
21				22			
23				24			
25				26			
27				28			
29				30			
31				32			
33				34			
35				36			
37				38			
39				40			
41				12			
13				11			

PJ

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01				02			
03				01			
05				06			
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			
21				22			
23				24			
25				26			

PJ

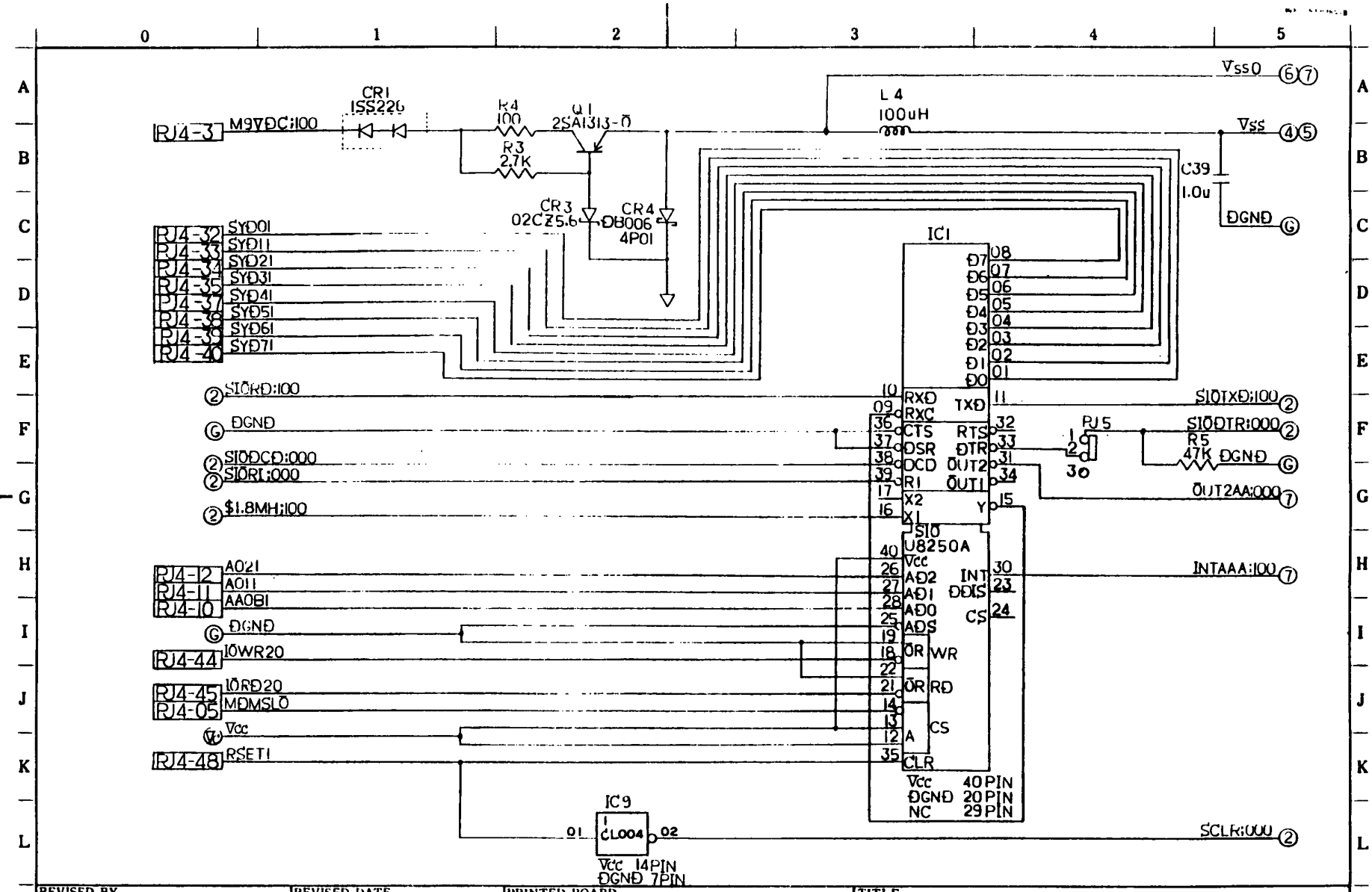
PIN	SIG. NAME	I/O	SH	PIO	SIG. NAME	I/O	SH
01				02			
03				01			
05				06			
07				08			

PJ

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01				02			
03				04			
05				06			
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			

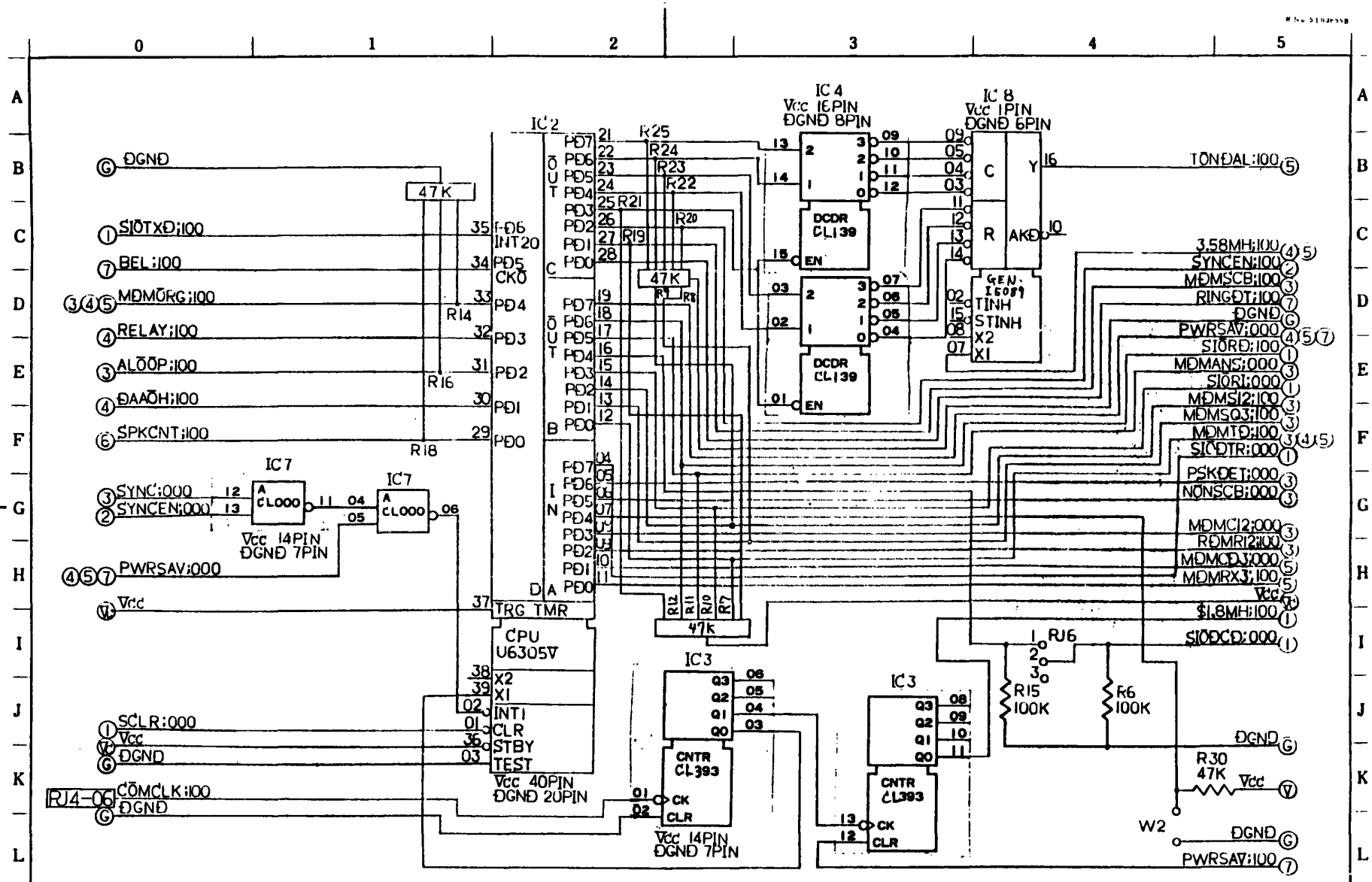
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE	CONNECTOR PIN SIGNAL MAP 2	
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No	DRAWING No.	PAGE No 3 / REV. MARK A

TOSHIBA CORPORATION



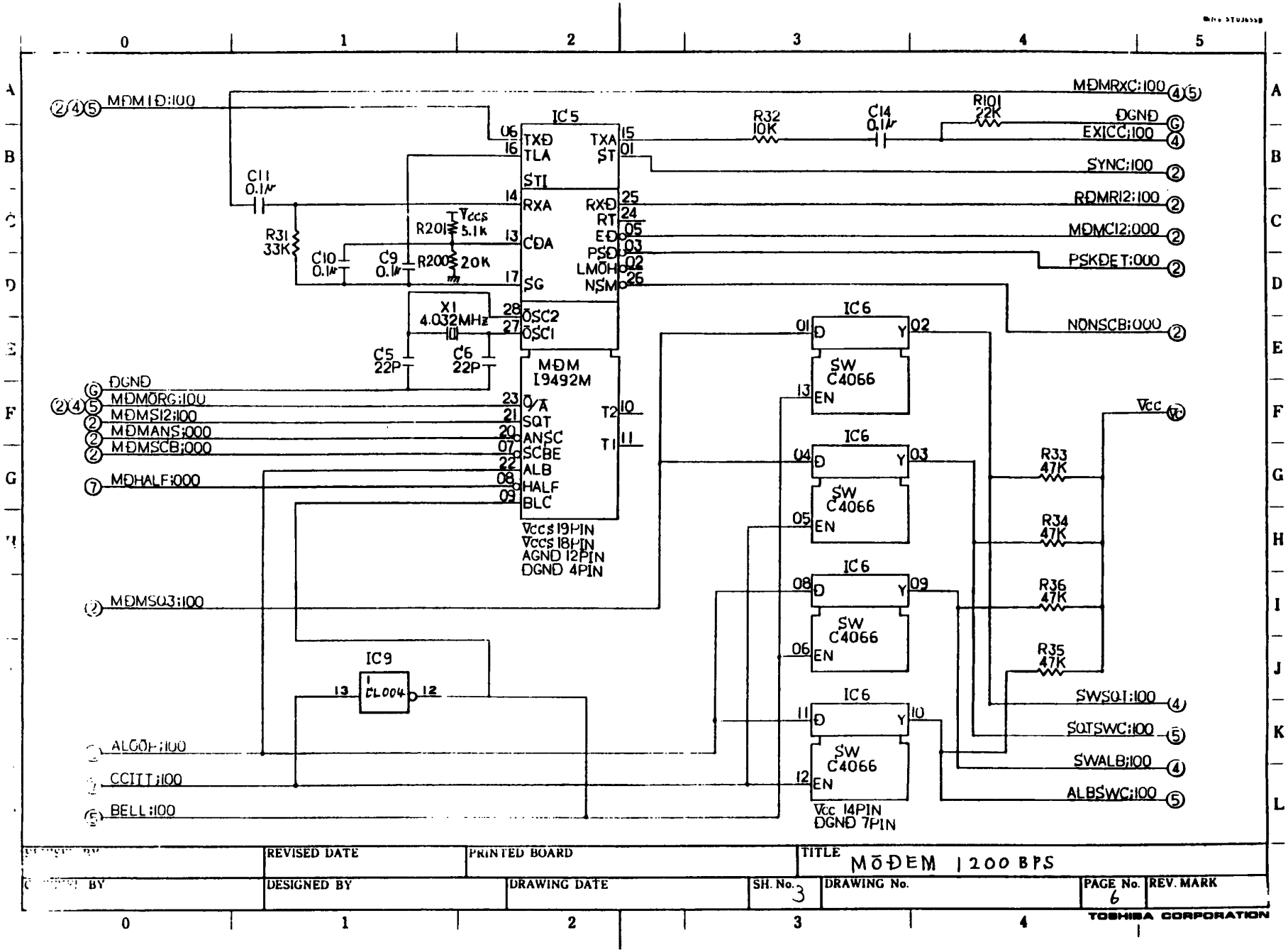
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE SIŌ(UART)/SESTEMINTERFACE			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 1	DRAWING No.	PAGE No. 4	REV. MARK A

TOSHIBA CORPORATION



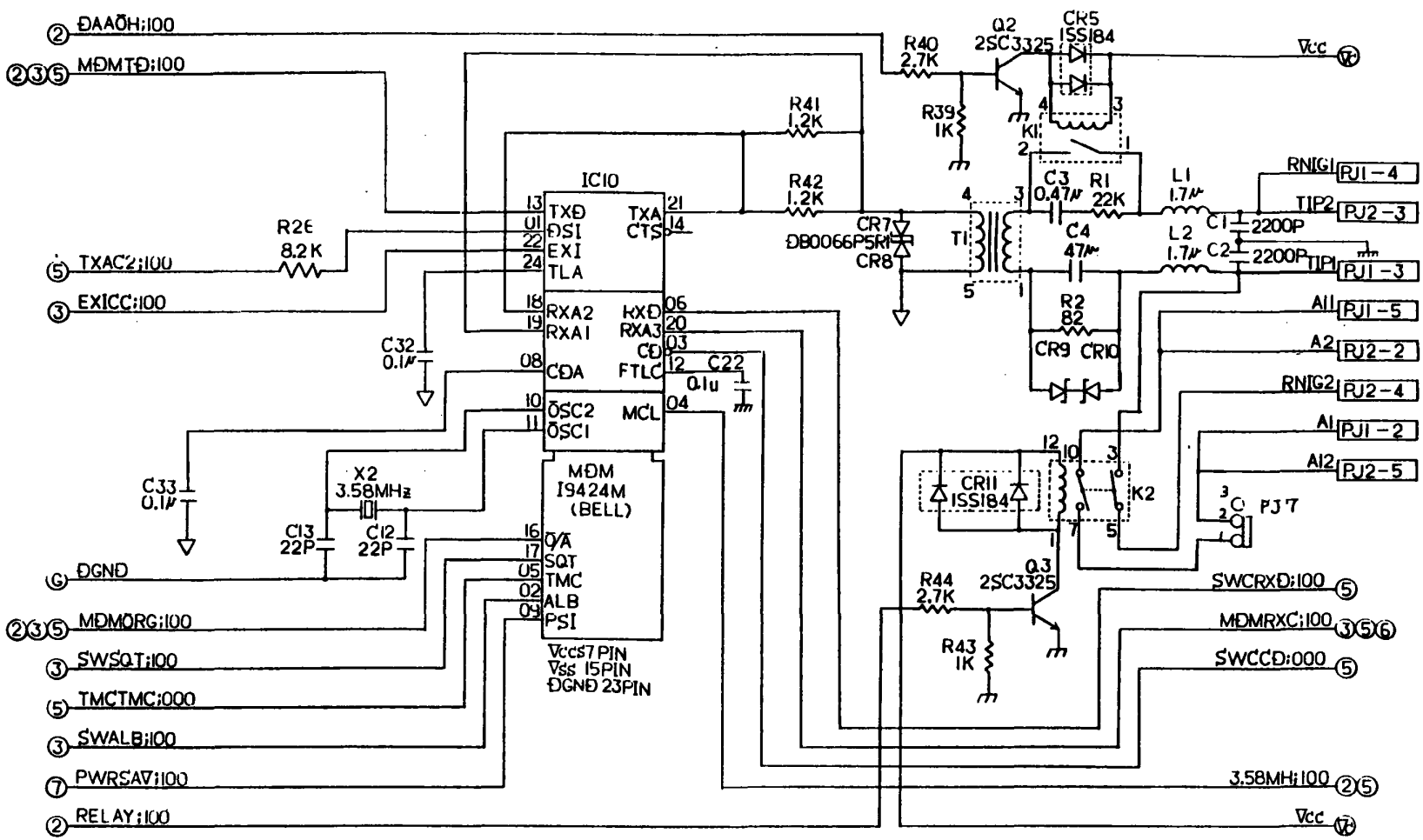
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE CPU
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 2 / DRAWING No. / PAGE No. 5 / REV. MARK A

TOSHIBA CORPORATION



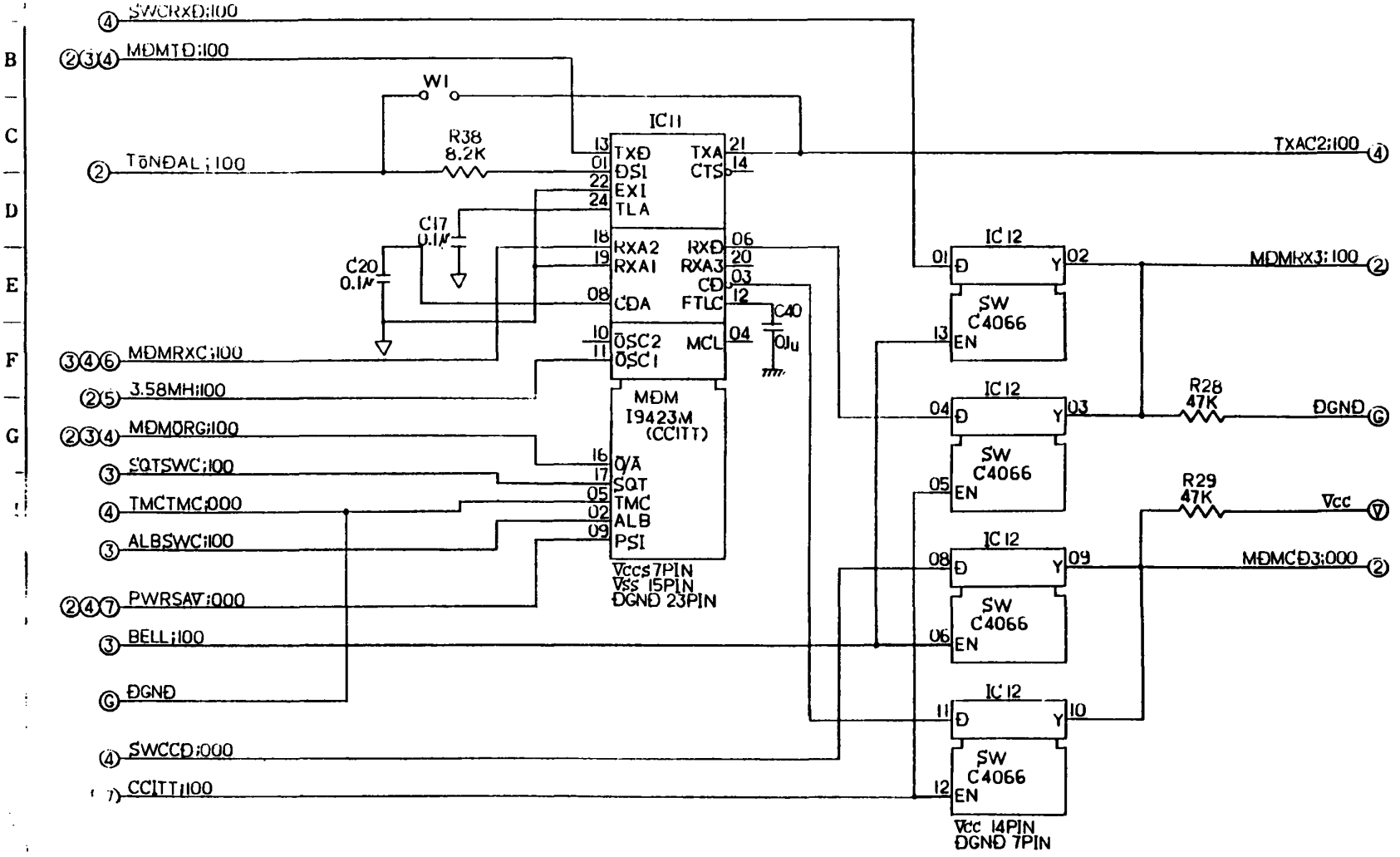
	REVISED DATE	PRINTED BOARD	TITLE MODEM 1200 BPS			
BY	DESIGNED BY	DRAWING DATE	SH. No. 3	DRAWING No.	PAGE No. 6	REV. MARK

TOSHIBA CORPORATION



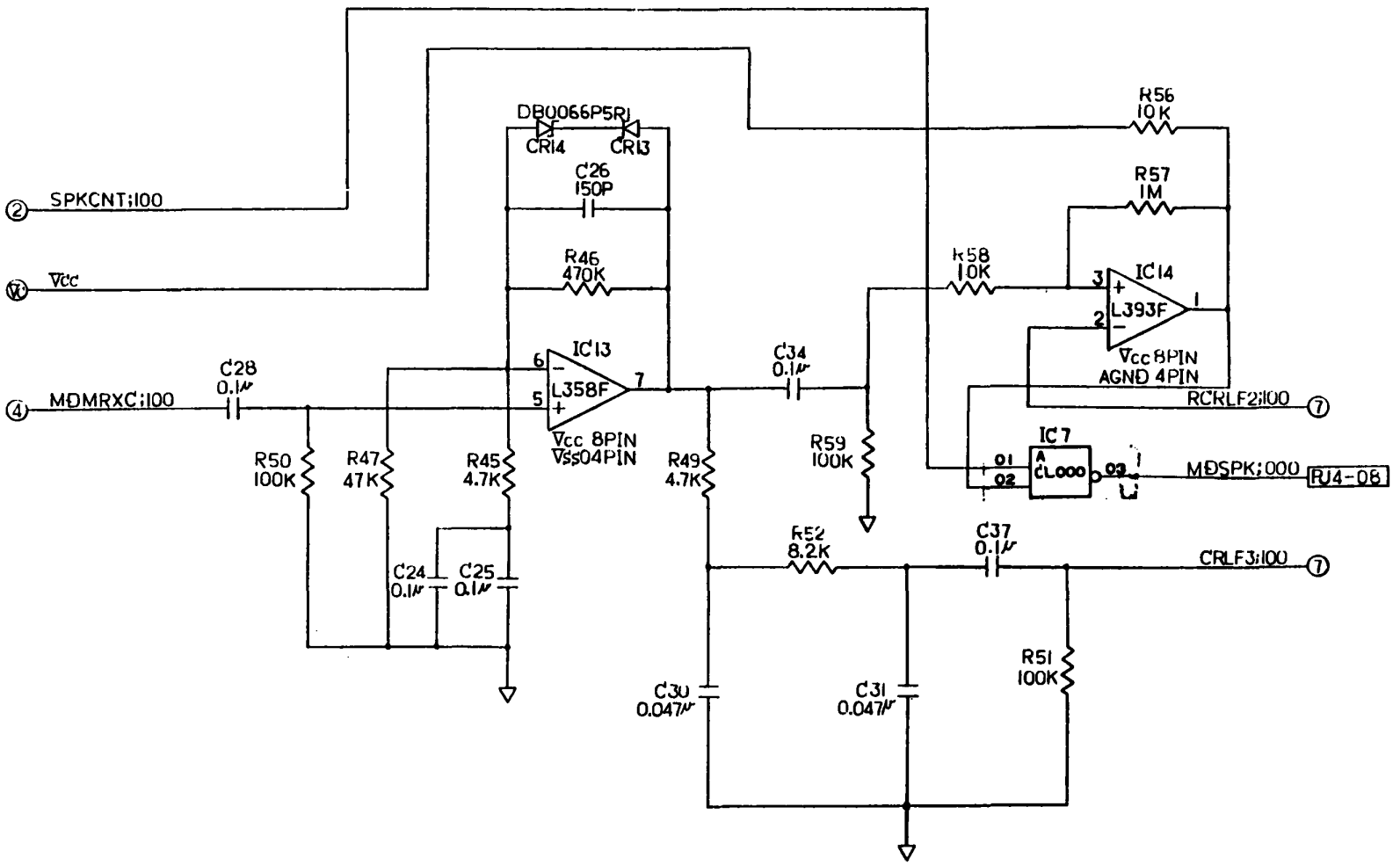
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE MÕĐEM 300BPS CCITT
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 4 / DRAWING No. / PAGE No. 7 / REV. MARK B

TOSHIBA CORPORATION



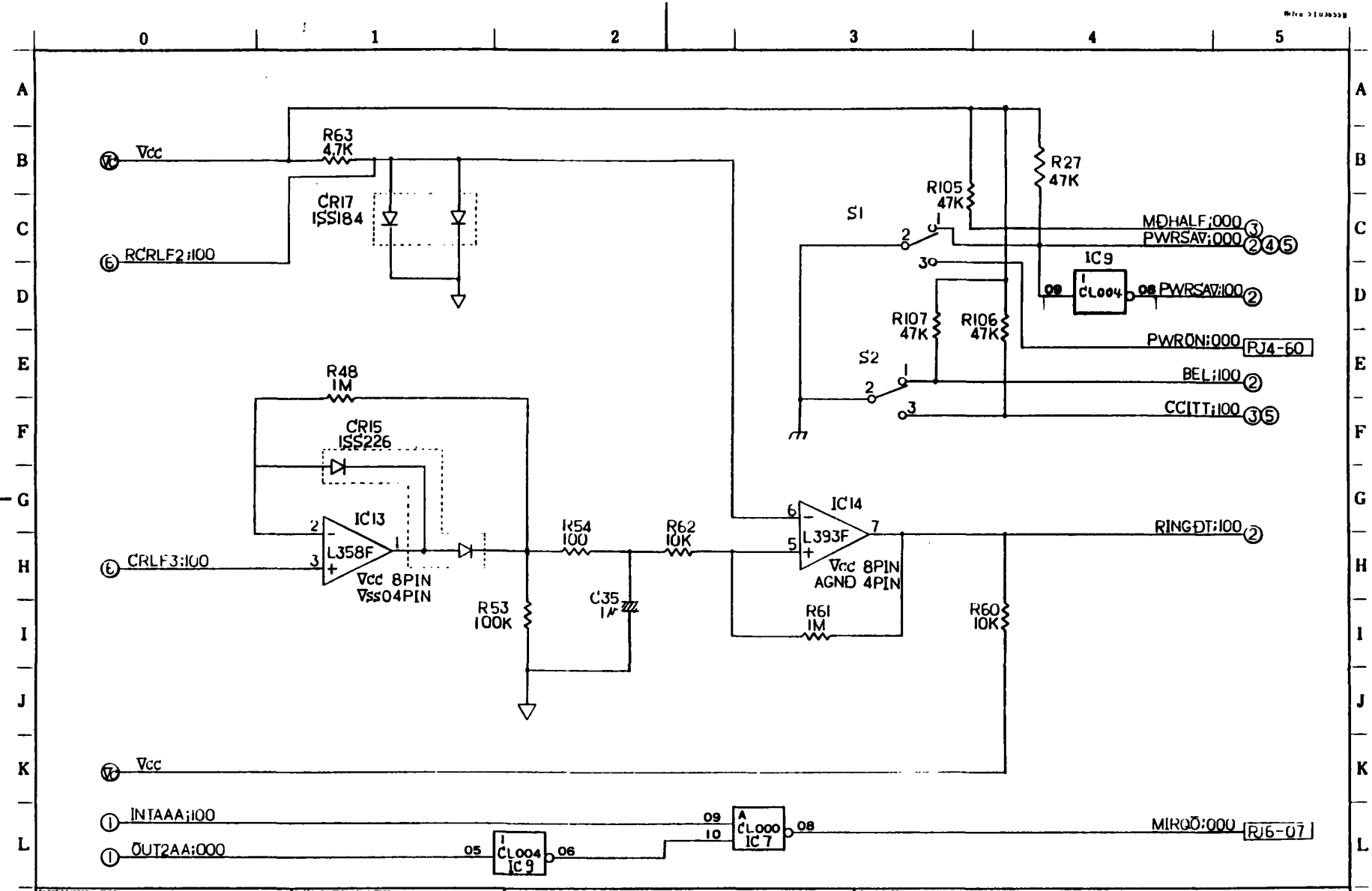
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE MODEM 300BPS BELL			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 5	DRAWING No.	PAGE No. 8	REV. MARK A

TOSHIBA CORPORATION



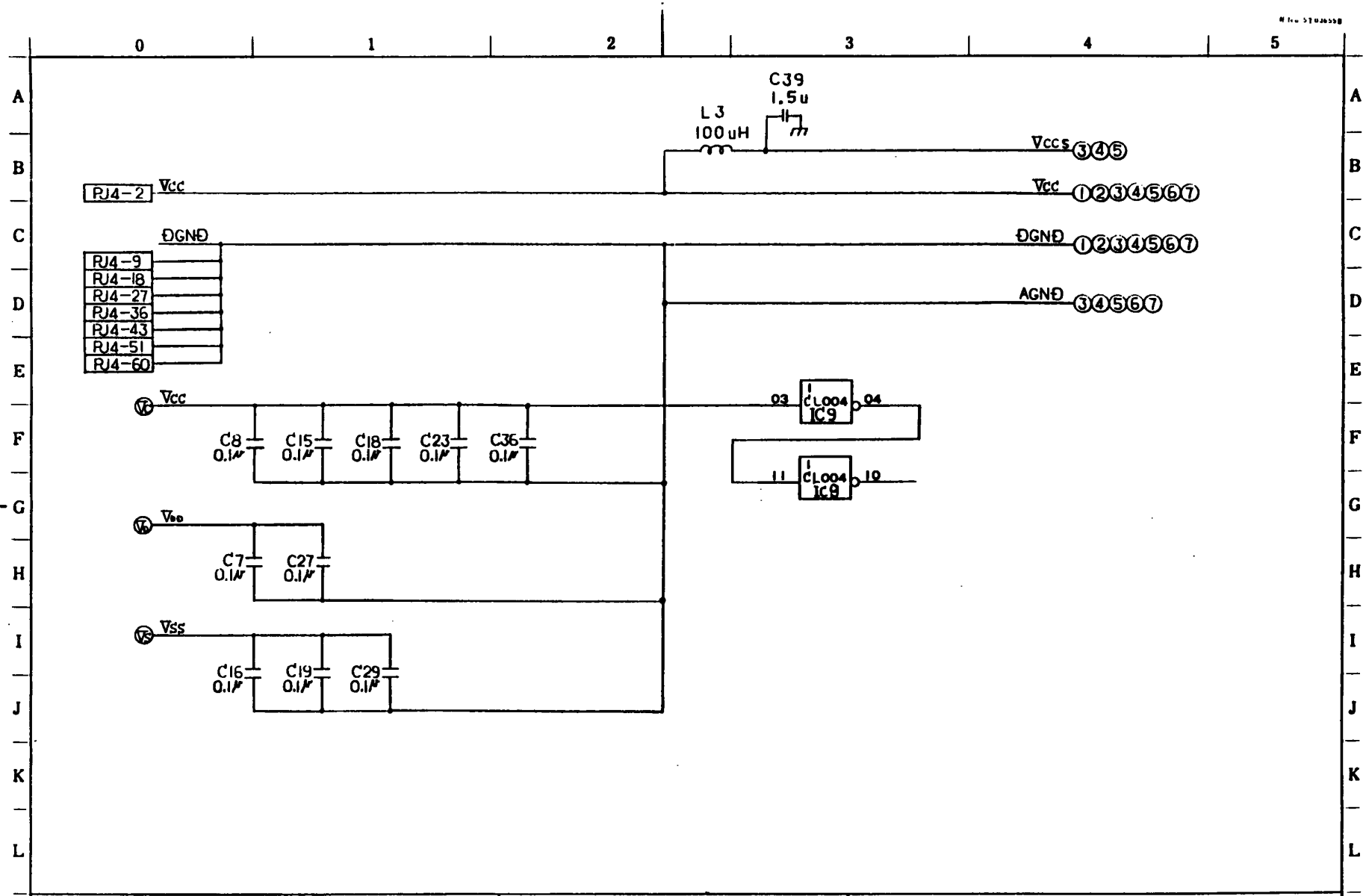
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE FILTER		
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 6	DRAWING No.	PAGE No. 9 / REV. MARK B

TOSHIBA CORPORATION



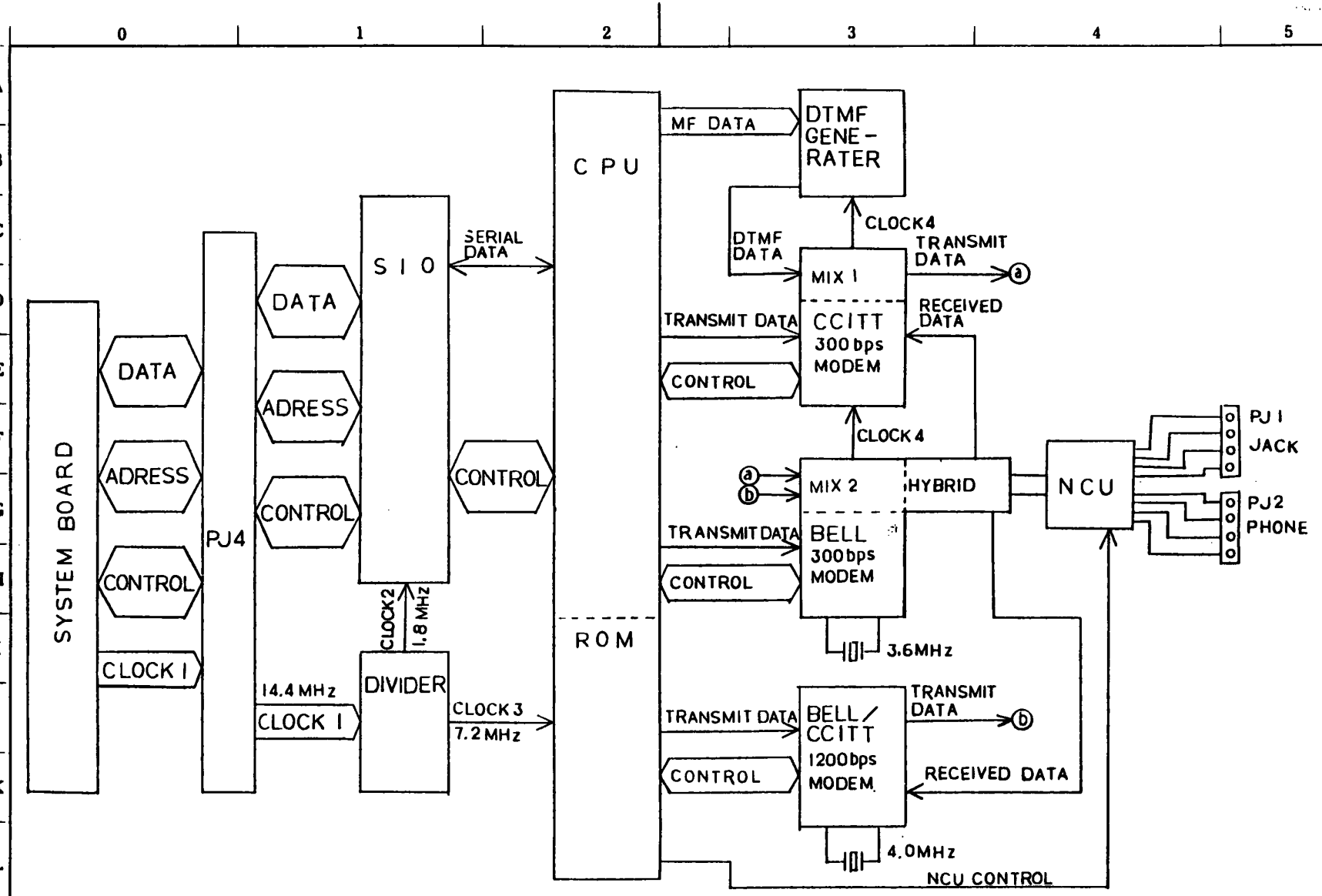
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE TONE DETECT			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 7	DRAWING No.	PAGE No. 10	REV. MARK A

TOSHIBA CORPORATION



REVISED BY	REVISED DATE	PRINTED BOARD	TITLE PASCON & AKIGATE			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 8	DRAWING No.	PAGE No. 11	REV. MARK A

TOSHIBA CORPORATION



REVISED BY	REVISED DATE	PRINTED BOARD	TITLE BLOCK DIAGRAM			
CHECKED BY	DESIGNED BY	DRAWING DATE	SII. No. 9	DRAWING No.	PAGE No. 12	REV. MARK A

TOSHIBA CORPORATION

展開接続図 SCHEMATIC DIAGRAMS

1200 bps MODEM CARD

F12MD3

変更回数 REV.MARK	記事 CONTENTS	承認 APPROVED BY	担当 REVISED BY	保管 REGISTERED
A	ISSUE	J. Makino '86.5.7	[illegible]	[illegible]
B	変更 7, 9 頁	J. Makino '86.6.4	K. Kaji '86.6.4	. .
		. .	. .	. .
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株式会社 東芝
TOSHIBA CORPORATION

承認 APPROVED BY	検図 CHECKED BY	設計 DESIGNED BY	図面番号 DRAWING NO	変更回数 REV MARK
J. Makino [illegible]	. .	[illegible]	34M900099	E

品名記号 CODE

TOTAL 12 CONT ON PAGE NO

PJ 4 SYSTEM INTERFACE

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	N			02	VCC		8
03	MPUDC	O	1	04	NC		
05	MPUSLO	I		06	COMCLK1	I	2
07	MIRQ5;000	O	7	08	MDSPk;000	O	6
09	DGND		8	10	AA0B1	I	1
11	A011	I	1	12	A021	I	1
13	NC			14	NC		
15	NC			16	NC		
17	NC			18	DGND		8
19	NC			20	NC		
21	N			22	NC		
23	NC			24	NC		
25	NC			26	NC		
27	DGND		8	28	NC		
29	NC			30	NC		
31	NC			32	SYD01	O	1
33	SYD11	O	1	34	SYD21	O	1
35	SYD31	O	1	36	DGND		8
37	SYD41	O	1	38	SYD51	O	1
39	SYD61	O	1	40	SYD71	O	1
41	NC			42	NC		
43	DGND		8	44	IOWR20	I	1
45	IORD20	I	1	46	NC		
47	NC			48	RSET1	I	1
49	NC			50	NC		
51	DGND		8	52	NC		
53	NC			54	NC		
55	NC			56	NC		
57	NC			58	NC		
59	NC			60	SYSCNT;000	O	7

PJ 1 TELEPHONE 1

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	NC			02	A1	I/O	4
03	TIP1	I/O	4	01	RING1	I/O	4
05	A11	I/O	4	06	NC		
07				08			
09				10			
11				12			
13				11			
15				16			
17				18			
19				20			
21				22			
23				24			
25				26			
27				28			
29				30			
31				32			
33				34			
35				36			
37				38			
39				40			
41				42			
43				44			

PJ 2 TELEPHONE 2

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	NC			02	A2	I/O	4
03	TIP2	I/O	4	01	RING2	I/O	4
05	A12	I/O	4	06	NC		
07				08			
09				10			
11				12			
13				11			
15				16			
17				18			
19				20			
21				22			
23				24			
25				26			

PJ 5 DTR CONTROL

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	SIODTR;000	O	1	02	DTR	O	1
03	NC		2	01			
05				06			
07				08			

PJ 6 CD CONTROL

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	PD4	O	2	02	SIODCD;000	I	2
03	NC		2	01			
05				06			
07				08			
09				10			
11				12			
13				11			
15				16			
17				18			
19				20			

REVISED BY	REVISED DATE	PRINTED BOARD	TITLE	CONNECTOR PIN SIGNAL MAP
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No	DRAWING No	PAGE No 2	REV MARK A

TOSHIBA CORPORATION

PJ7 LINE CONTROL

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	LINE 1	I/O	4	02	LINE 2	I/O	4
03	NC		4	04			
05				06			
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			
21				22			
23				24			
25				26			
27				28			
29				30			
31				32			
33				34			
35				36			
37				38			
39				40			
41				42			
43				44			
45				46			
47				48			
49				50			

PJ

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01				02			
03				04			
05				06			
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			
21				22			
23				24			
25				26			
27				28			
29				30			
31				32			
33				34			
35				36			
37				38			
39				40			
41				42			
43				44			

PJ

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01				02			
03				04			
05				06			
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			
21				22			
23				24			
25				26			

PJ

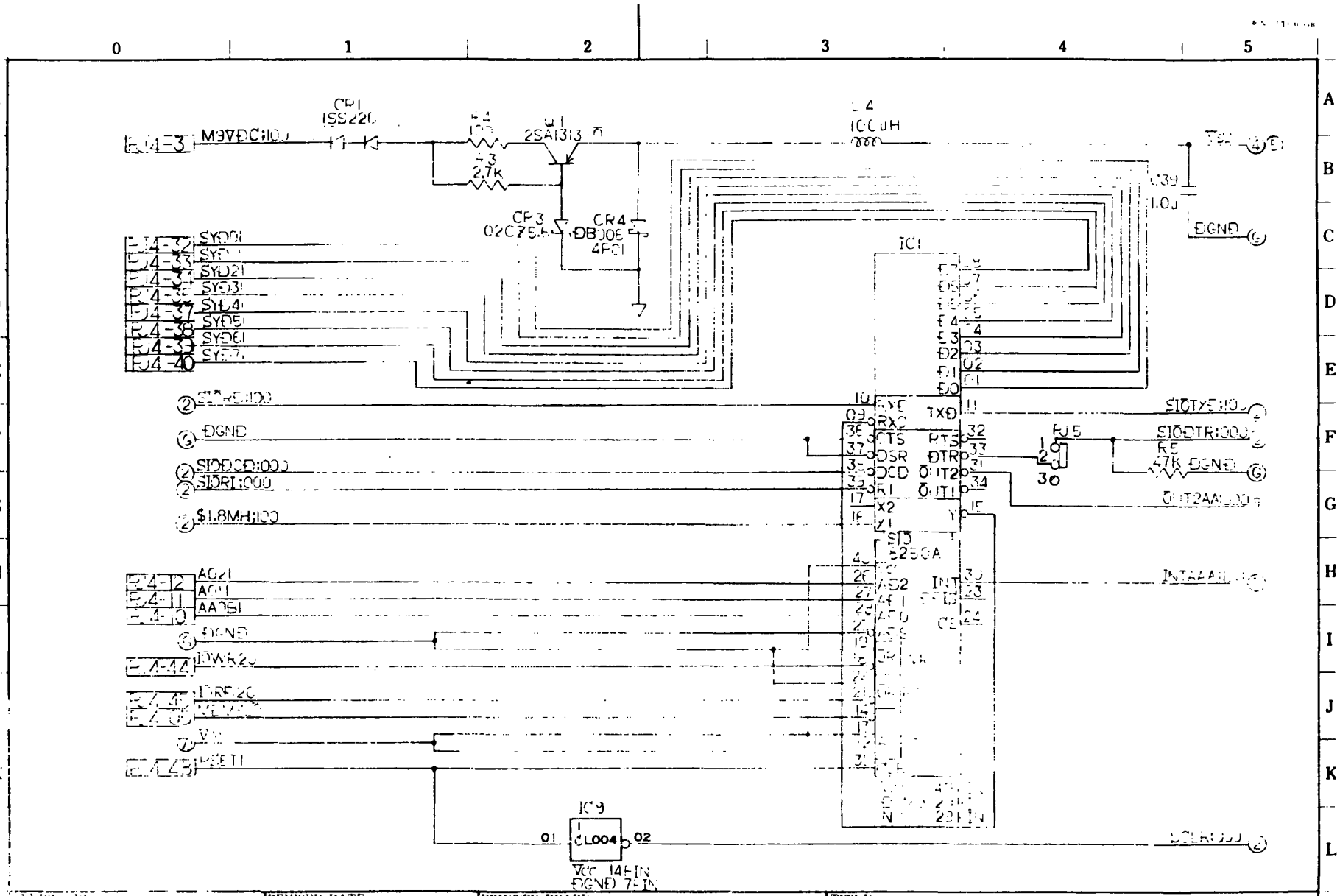
PIN	SIG. NAME	I/O	SH	PIO	SIG. NAME	I/O	SH
01				02			
03				04			
05				06			
07				08			

PJ

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01				02			
03				04			
05				06			
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			

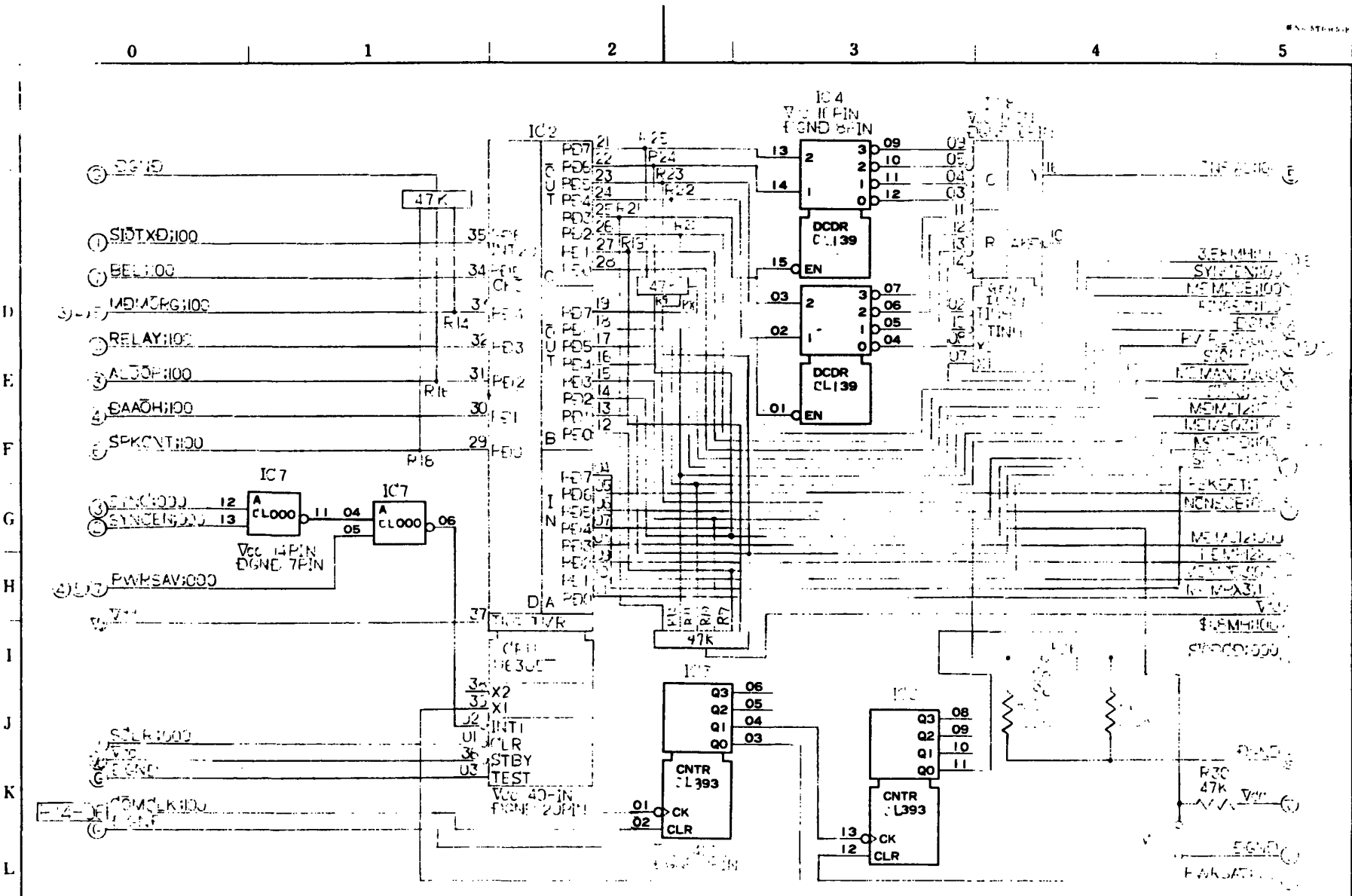
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE	CONNECTOR PIN SIGNAL MAP
DESIGNED BY	DESIGNED BY	DRAWING DATE	SH No	DRAWING No / PAGE No 3 / REV MARK

TOSHIBA CORPORATION



REVISED BY	REVISED DATE	PRINTED BOARD	TITLE SIO(UART)/SESTEMINTERFACE				
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No. 1	DRAWING No	PAGE No. 4	REV. MARK A	

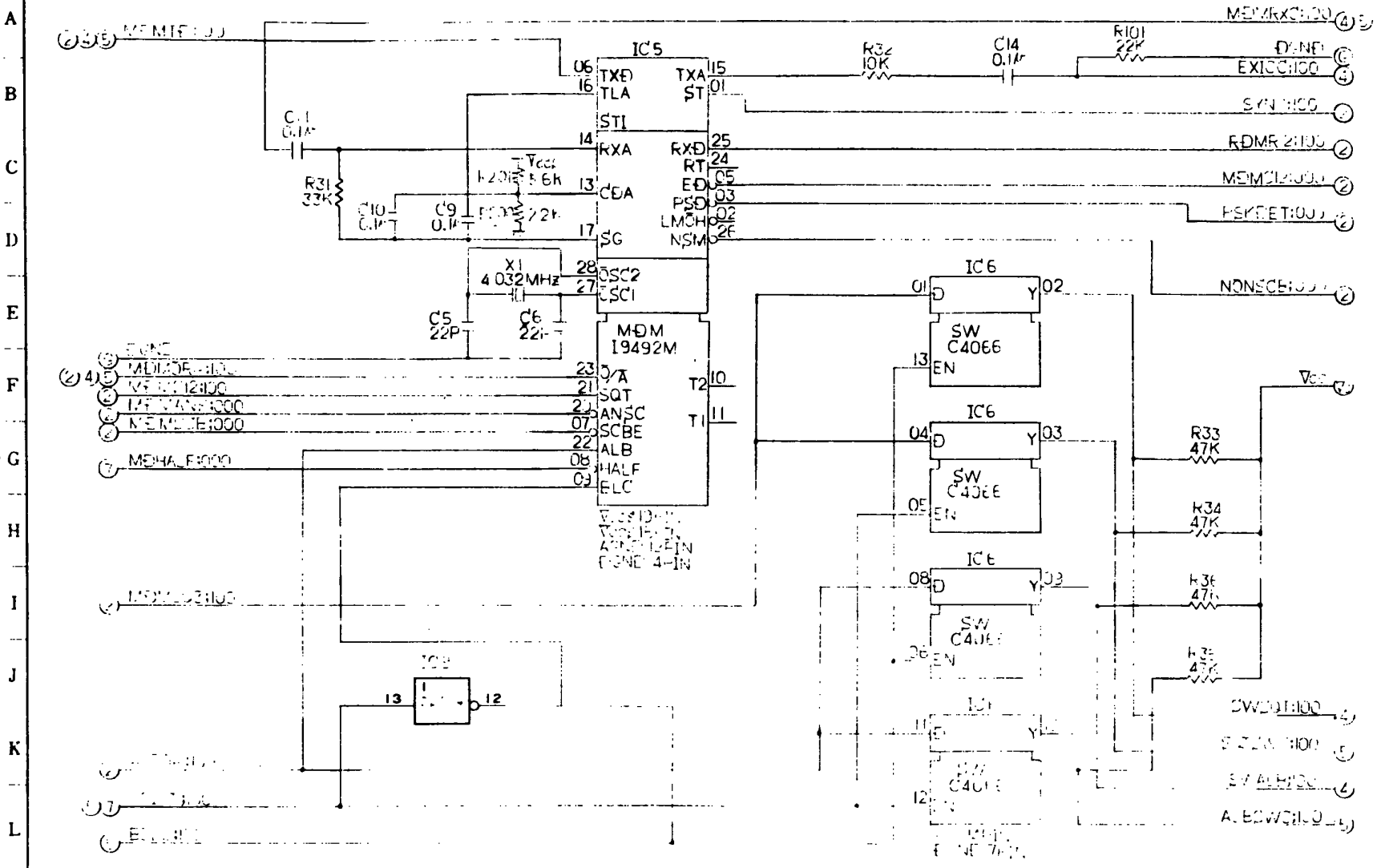
TOSHIBA CORPORATION



REVISED BY	REVISED DATE	PRINTED BOARD	TITLE C P U	
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No. 2	DRAWING No.

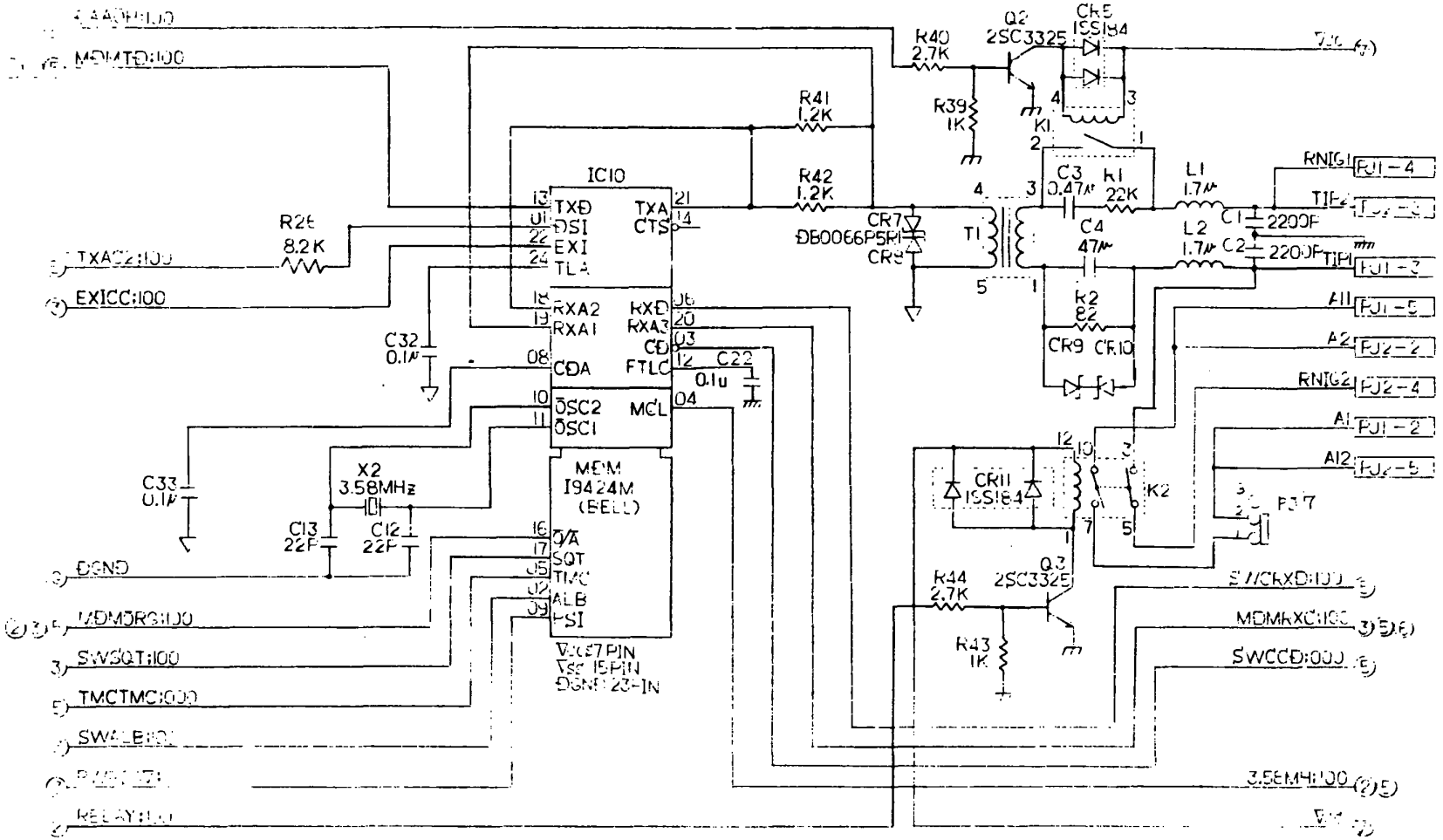
PAGE No. 5 REV MARK /

TOSHIBA CORPORATION



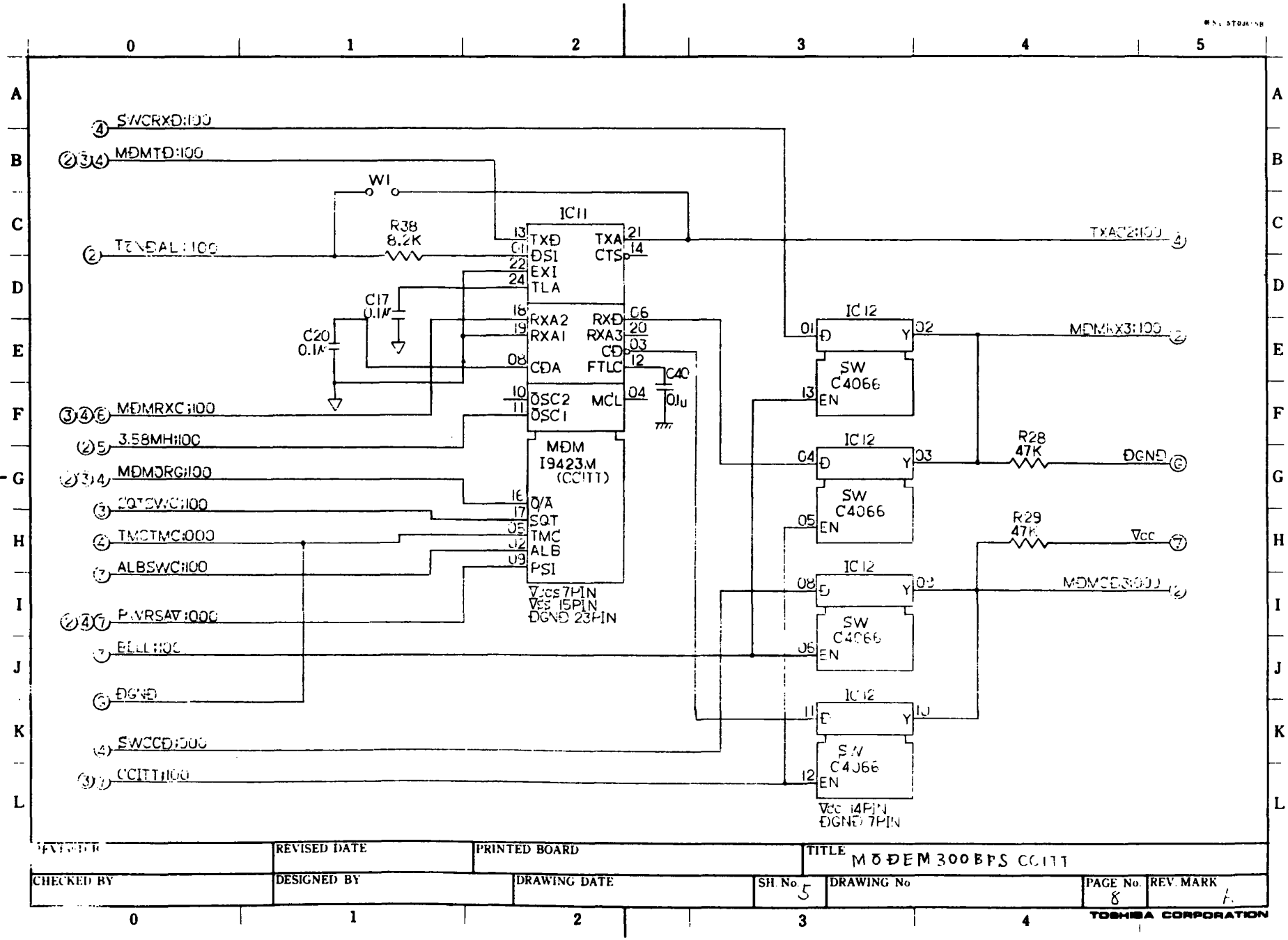
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE MODEM 12001 BT
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No 3 / DRAWING No / PAGE No 6 / REV MARK

TOSHIBA CORPORATION



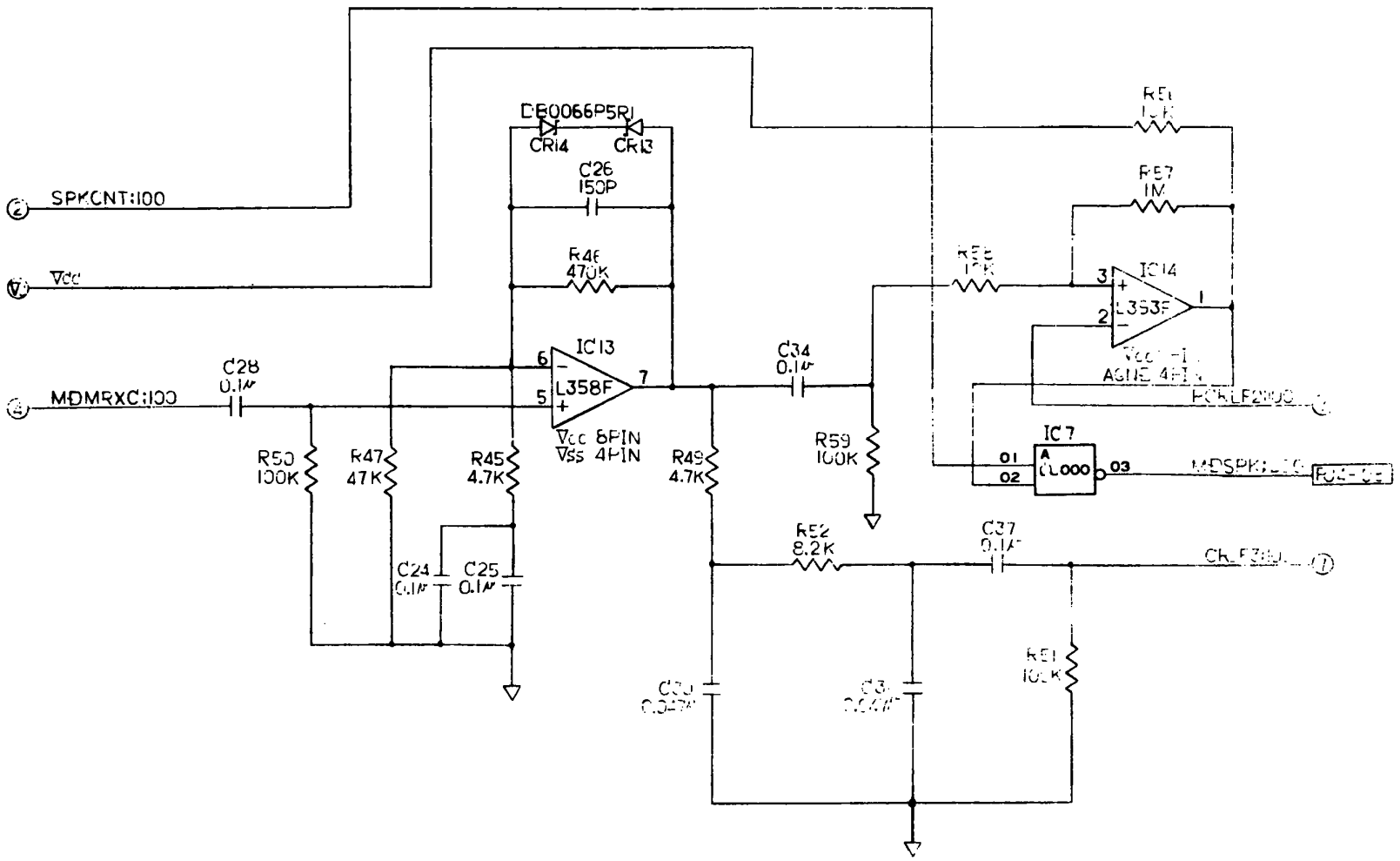
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE MODEM 300BPS BE...
APPROVED BY	DESIGNED BY	DRAWING DATE	SH No 4 / DRAWING No / PAGE No / REV MARK

TOSHIBA CORPORATION



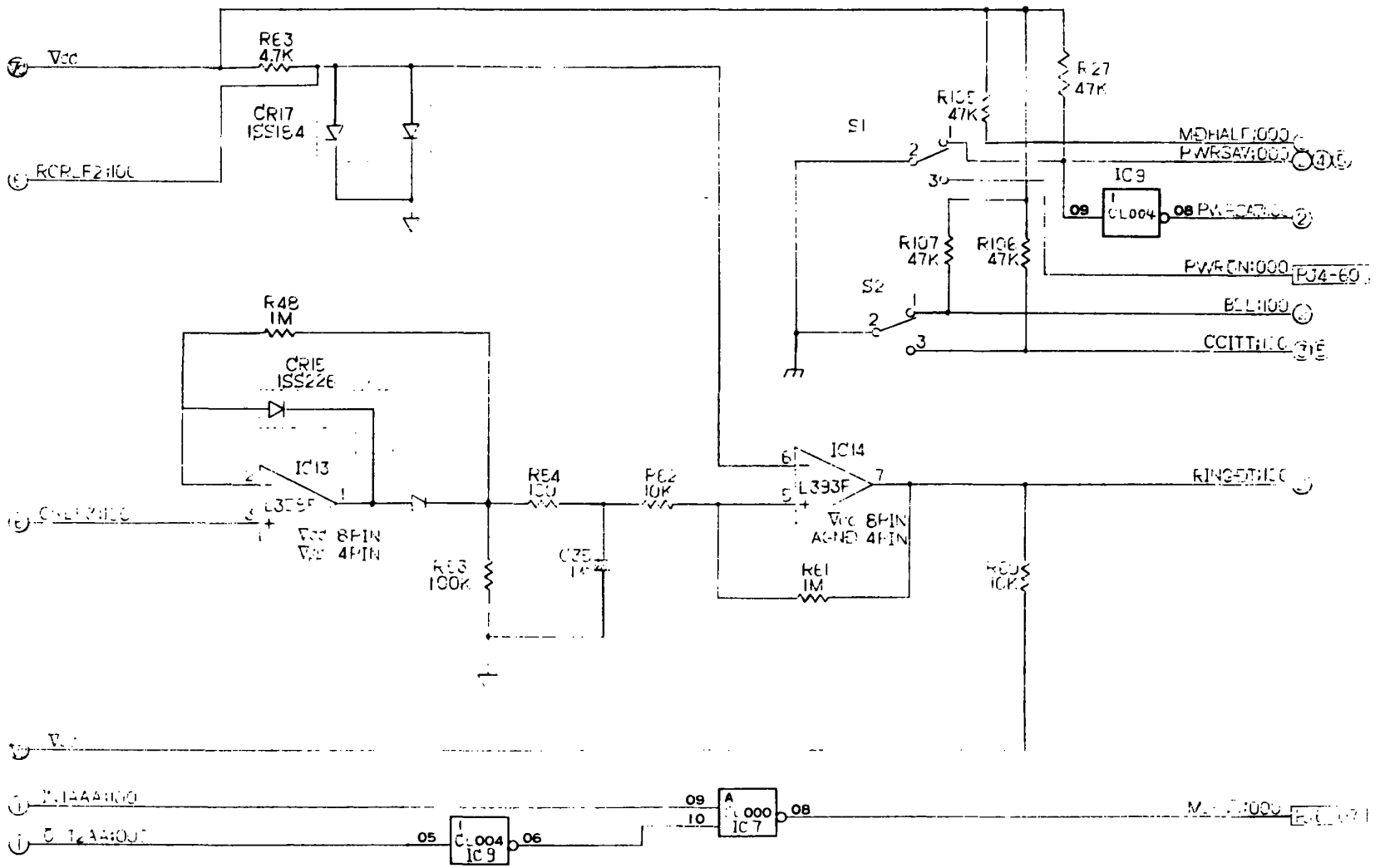
PATENTED	REVISED DATE	PRINTED BOARD	TITLE MODEM 300BPS CCITT			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 5	DRAWING No	PAGE No. 8	REV. MARK A

TOSHIBA CORPORATION



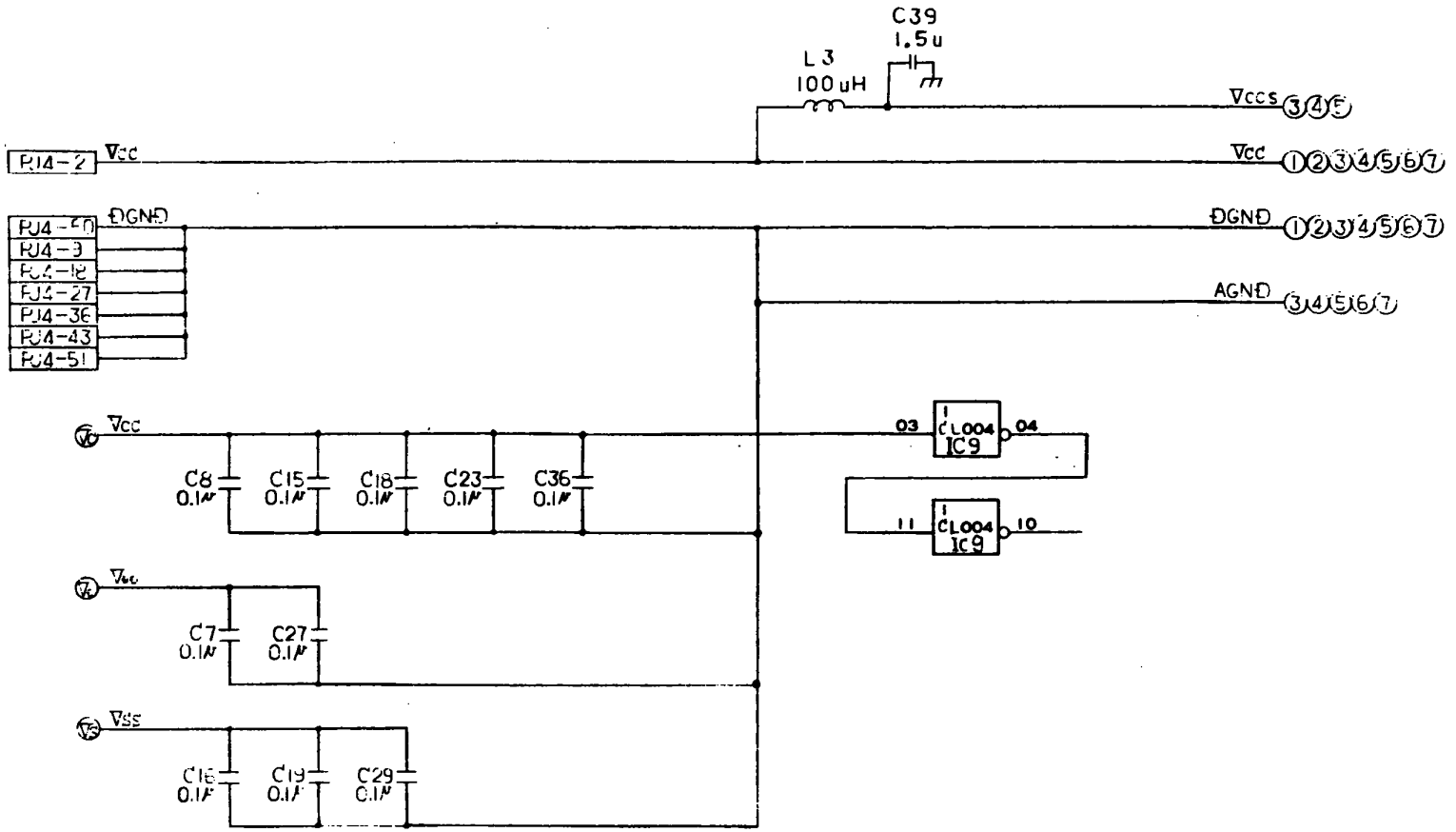
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE FILTER			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No 6	DRAWING No	PAGE No 9	REV MARK

TOSHIBA CORPORATION



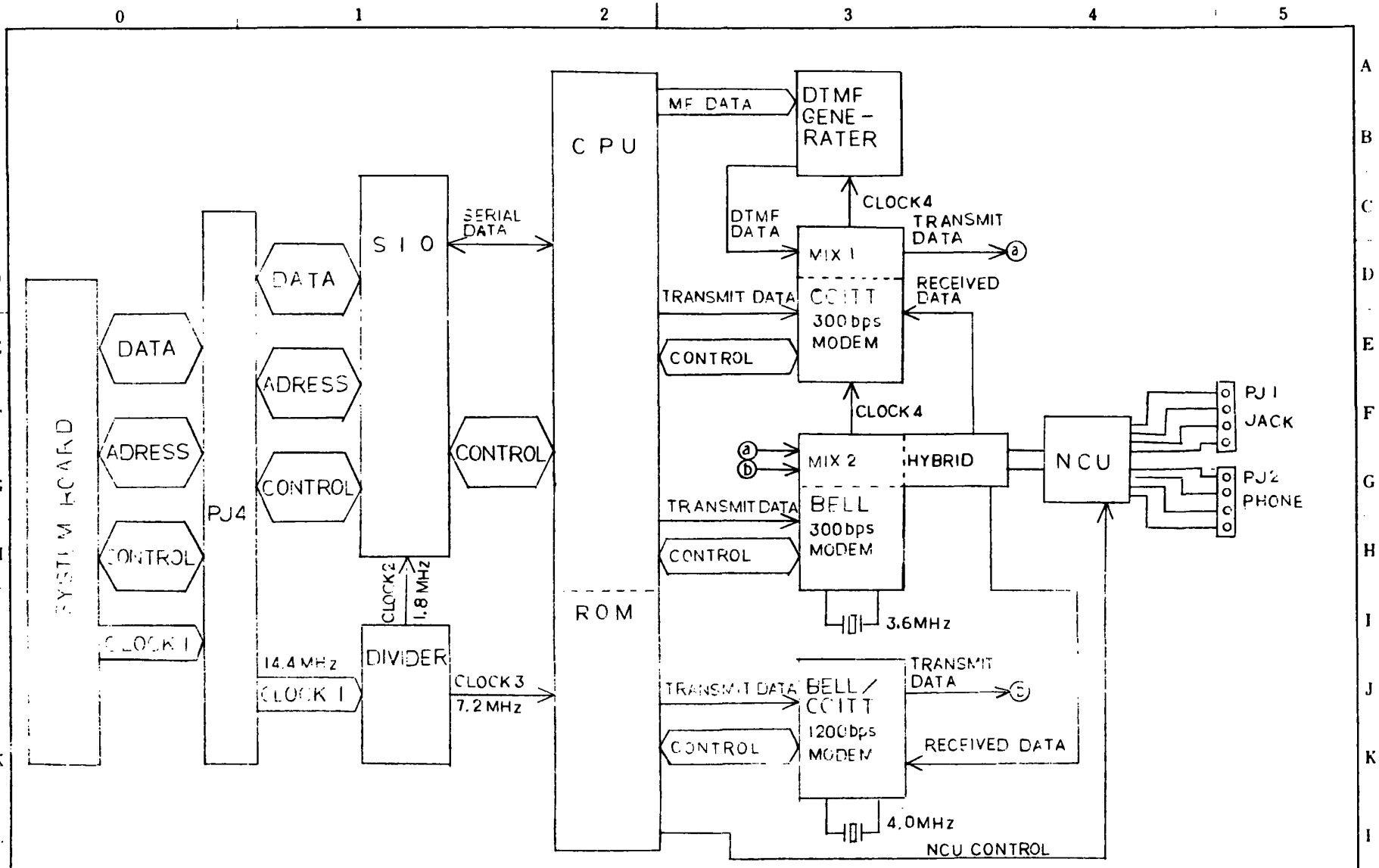
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE TONE DETECT				
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No. 1	DRAWING No.	PAGE No. 19	REV MARK L	

TOSHIBA CORPORATION



REVISED BY	REVISED DATE	PRINTED BOARD	TITLE PASCON & AKIGATE			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No 8	DRAWING No	PAGE No 11	REV MARK

TOSHIBA CORPORATION



REVISED BY	REVISED DATE	PRINTED BOARD	TITLE BLOCK DIAGRAM			
DESIGNED BY	DRAWING DATE	SH No. 9	DRAWING No.	PAGE No. 12	REV MARK	

TOSHIBA CORPORATION

展開接続図 SCHEMATIC DIAGRAMS

T2100

F12MD1

MODEM BOARD

34P710721G01

変更回数 REV.MARK	記事 CONTENTS	承認 APPROVED BY	担当 REVISED BY	保管 REGISTERED
A	ISSUE	T.Makino '86.2.4	Y.Miyama '86.2.4	S. Nakada '86.3.5
B	変更 全頁	T. Makino '87.3.31	Y. Miyama '86.2.31	A. Takahashi '86.4.2
C	変更 2,6,9頁	T.Makino '86.6.4	K.Kayi '87.6.3	..
		..	..	..
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承認 APPROVED BY	検図 CHECKED BY	設計 DESIGNED BY	図面番号 DRAWING NO.	変更回数 REV.MARK
	K.Kayi '87.2.4	.. '86.2.4	34M900013	C

品名記号 CODE

TOTAL 12 CONT. ON PAGE NO. 1

PJ4 SYSTEM INTERFACE

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	NC			02	VCC		8
03	MPWDC	O	1	04	NC		
05	MDMSLO	I		06	COMCLK1	I	2
07	MIRQ5;000	O	7	08	MDSPK;000	O	6
09	DGND		8	10	AA081	I	1
11	AD11	I	1	12	A021	I	1
13	NC			14	NC		
15	NC			16	NC		
17	NC			18	DGND		8
19	NC			20	NC		
21	NC			22	NC		
23	NC			24	NC		
25	NC			26	NC		
27	DGND		8	28	NC		
29	NC			30	NC		
31	NC			32	SYD01	O	1
33	SYD11	O	1	34	SYD21	O	1
35	SYD31	O	1	36	DGND		8
37	SYD41	O	1	38	SYD51	O	1
39	SYD61	O	1	40	SYD71	O	1
41	NC			42	NC		
43	DGND		8	44	IOWR20	I	1
45	IORD20	I	1	46	NC		
47	NC			48	RSET1	I	1
49	NC			50	NC		
51	DGND		8	52	NC		
53	NC			54	NC		
55	NC			56	NC		
57	NC			58	NC		
59	NC			60	DGND		8

PJ1 TELEPHONE 1

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	NC			02	A1	I/O	4
03	TIP1	I/O	4	04	RING1	I/O	4
05	A11	I/O	4	06	NC		
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			
21				22			
23				24			
25				26			
27				28			
29				30			
31				32			
33				34			
35				36			
37				38			
39				40			
41				42			
43				44			

PJ2 TELEPHONE 2

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	NC			02	A2	I/O	4
03	TIP2	I/O	4	04	RING2	I/O	4
05	A12	I/O	4	06	NC		
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			
21				22			
23				24			
25				26			

PJ5 DTR CONTROL

PIN	SIG. NAME	I/O	SH	PIO	SIG. NAME	I/O	SH
01	SIODTR;000	I	1	02	DTR	O	1
03	NC		2	04			
05				06			
07				08			

PJ6 CD CONTROL

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	PD4	O	2	02	SIODCD;000	I	2
03	NC		2	04			
05				06			
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			

REVISED BY	REVISED DATE	PRINTED BOARD	TITLE	CONNECTOR PIN SIGNAL MAP 1
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No.	DRAWING No. / PAGE No. 2 / REV. MARK C

TOSHIBA CORPORATION

PJ7 LINE CONTROL

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01	LINE 1	I/O	4	02	LINE 2	I/O	4
03	NC		4	04			
05				06			
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			
21				22			
23				24			
25				26			
27				28			
29				30			
31				32			
33				34			
35				36			
37				38			
39				40			
41				42			
43				44			
45				46			
47				48			
49				50			

PJ

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01				02			
03				04			
05				06			
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			
21				22			
23				24			
25				26			
27				28			
29				30			
31				32			
33				34			
35				36			
37				38			
39				40			
41				42			
43				44			

PJ

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01				02			
03				04			
05				06			
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			
21				22			
23				24			
25				26			

PJ

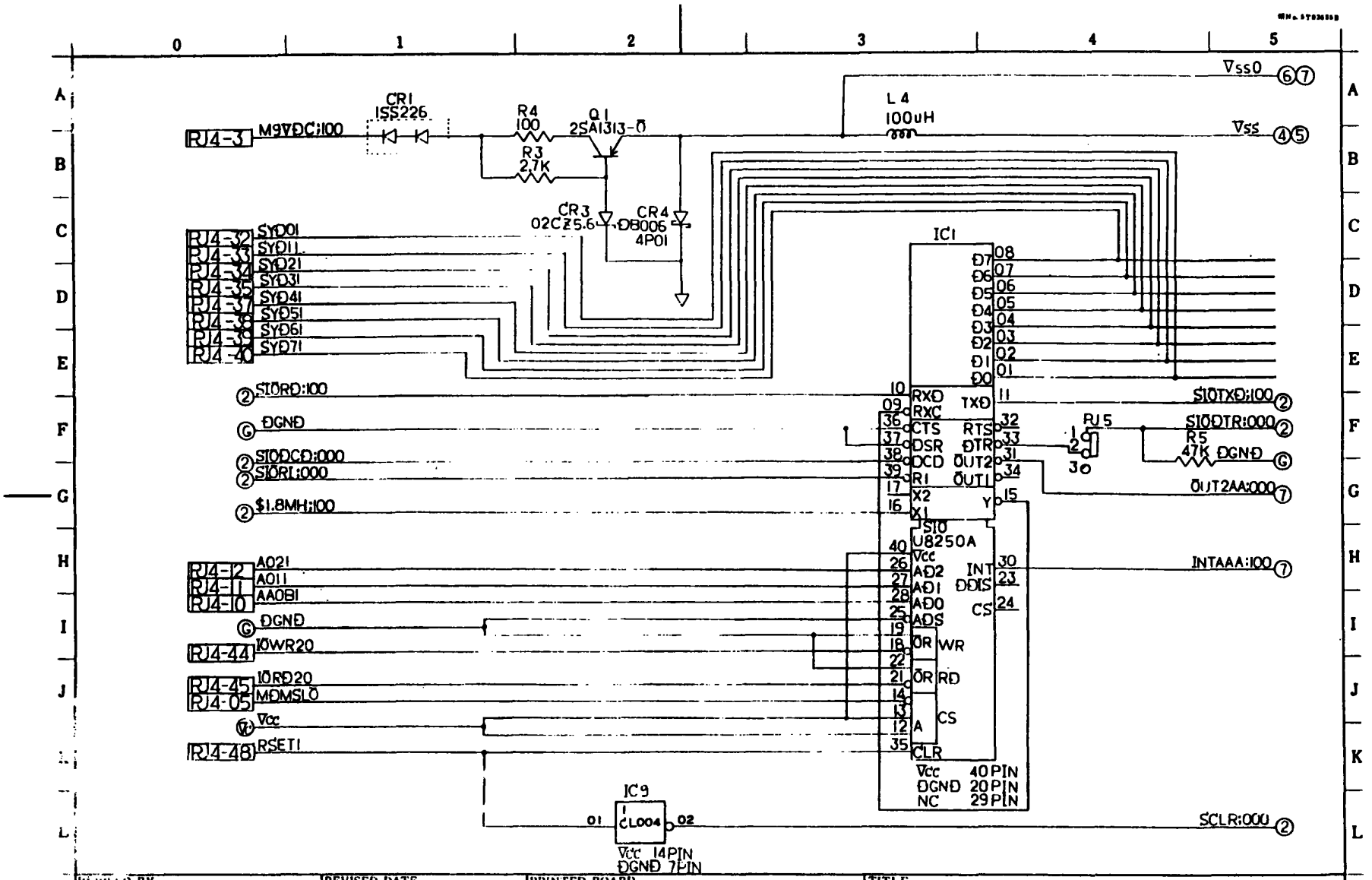
PIN	SIG. NAME	I/O	SH	PIO	SIG. NAME	I/O	SH
01				02			
03				04			
05				06			
07				08			

PJ

PIN	SIG. NAME	I/O	SH	PIN	SIG. NAME	I/O	SH
01				02			
03				04			
05				06			
07				08			
09				10			
11				12			
13				14			
15				16			
17				18			
19				20			

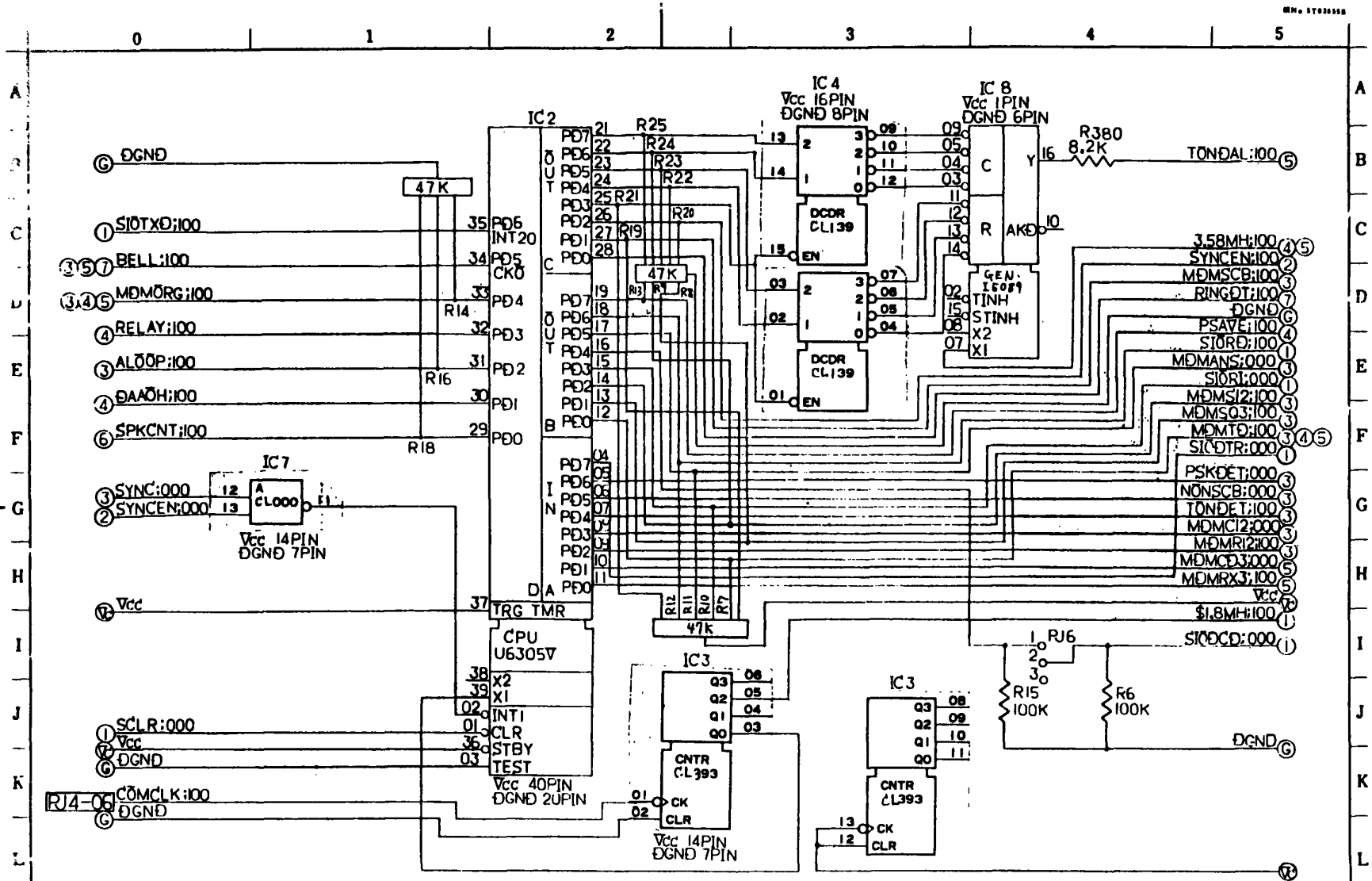
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE	CONNECTOR PIN SIGNAL MAP 2	
CHECKED BY	DESIGNED BY	DRAWING DATE	SH No.	DRAWING No.	PAGE No. 3 / REV. MARK B

TOSHIBA CORPORATION



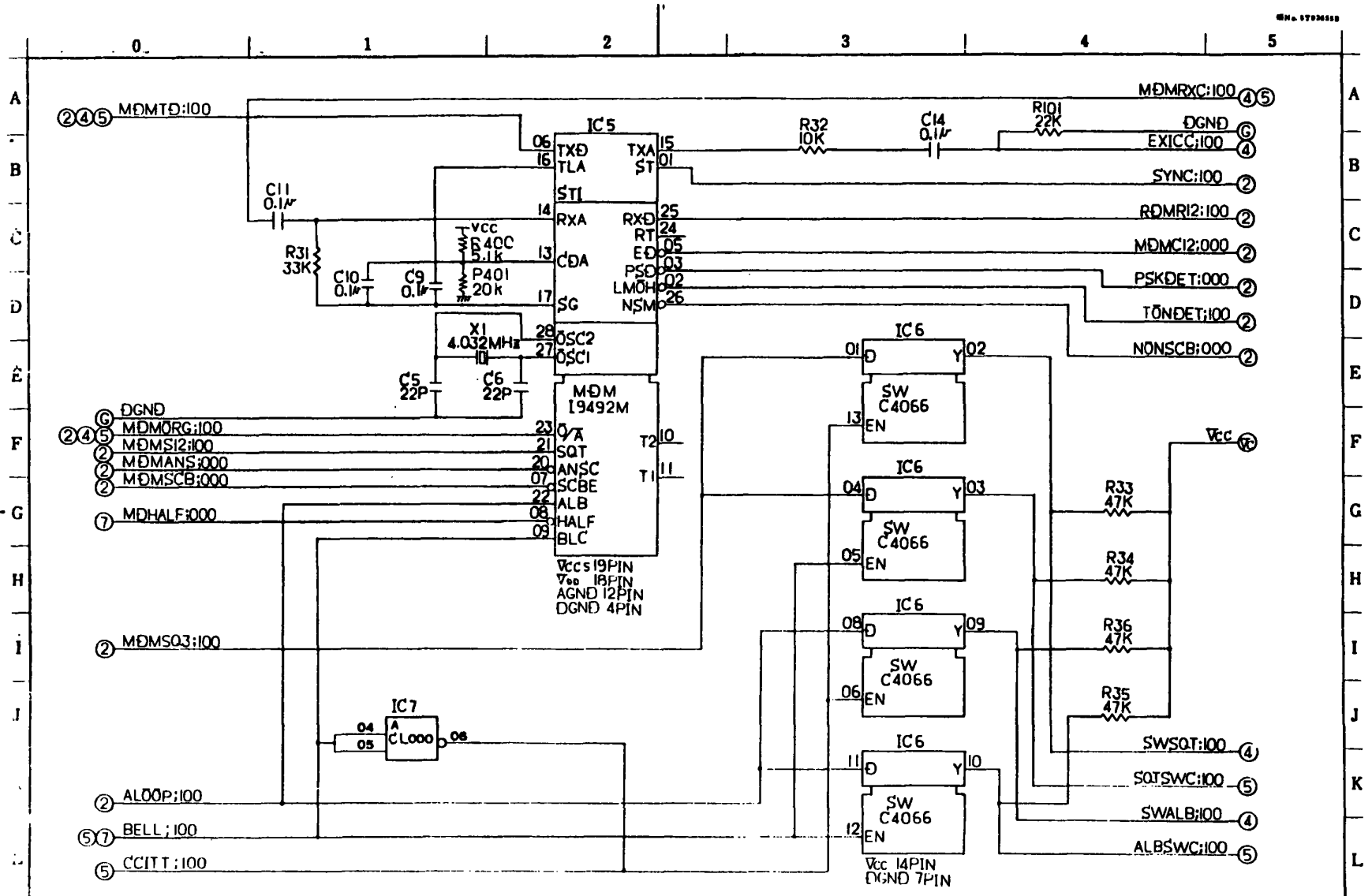
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE SIO(UART)/SESTEMINTERFACE			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 1	DRAWING No.	PAGE No. 4	REV. MARK B

TOSHIBA CORPORATION



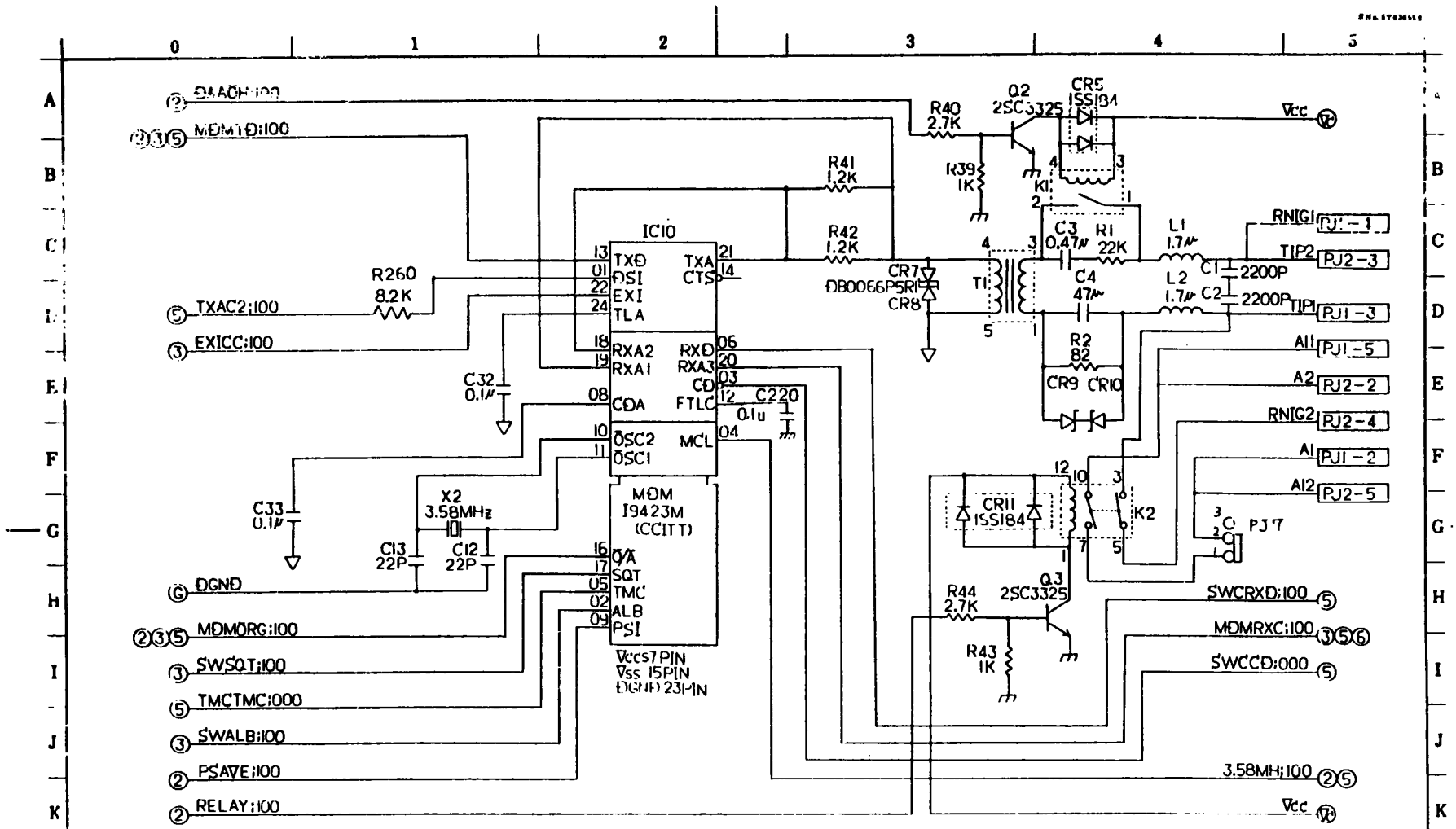
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE CPU			
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 2	DRAWING No.	PAGE No. 5	REV MARK B

TOSHIBA CORPORATION



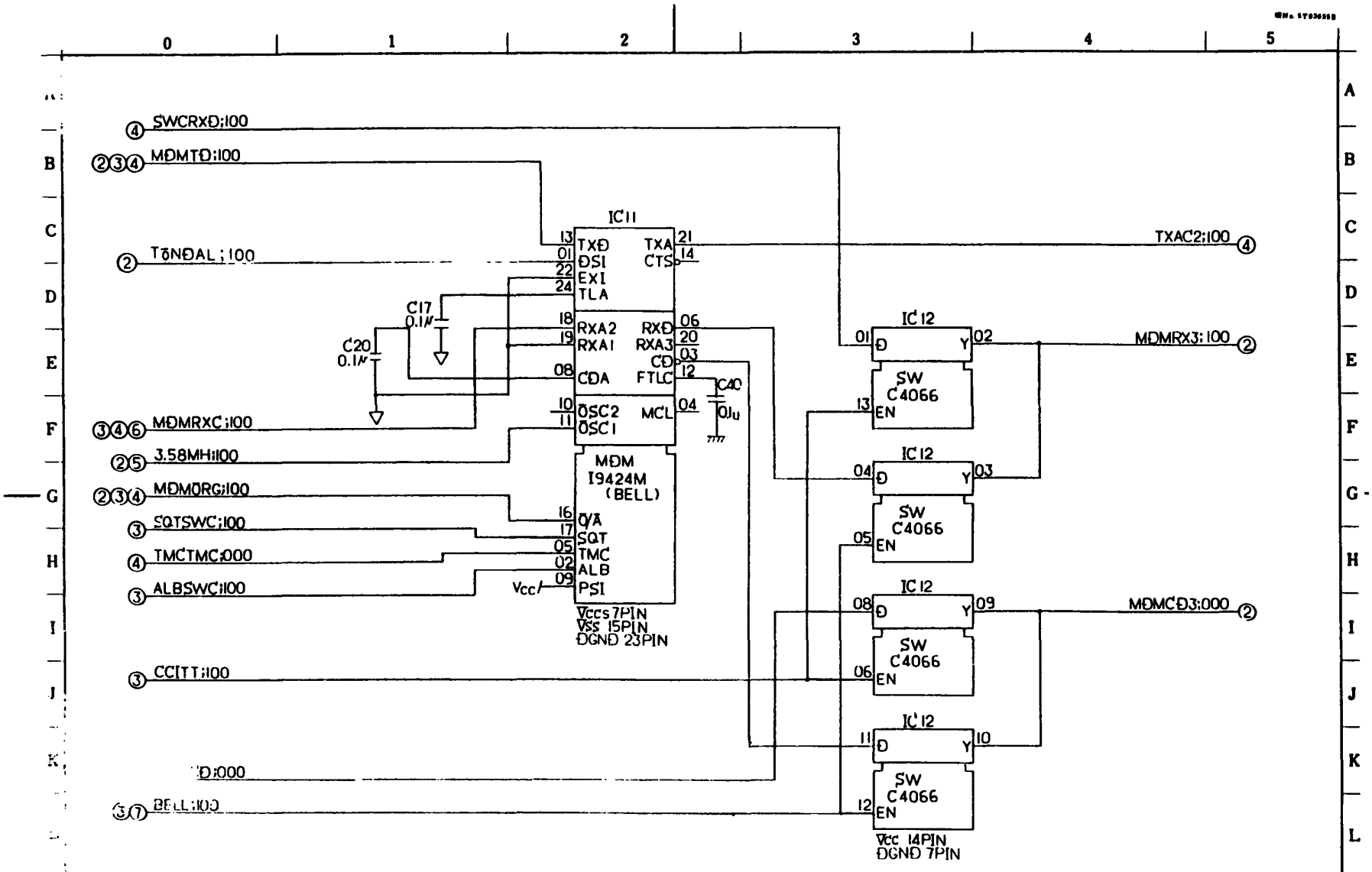
REVISED BY	REVISED DATE	PRINTED BOARD	TITLE MODEM 1200 BPS		
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 3	DRAWING No.	PAGE No. 6 / REV. MARK C

TOSHIBA CORPORATION



	REVISED DATE	PRINTED BOARD	TITLE MODEM 300BPS CCITT				
	DESIGNED BY	DRAWING DATE	SH No 4	DRAWING No	PAGE No 17	REV MARK B	

TOSHIBA CORPORATION



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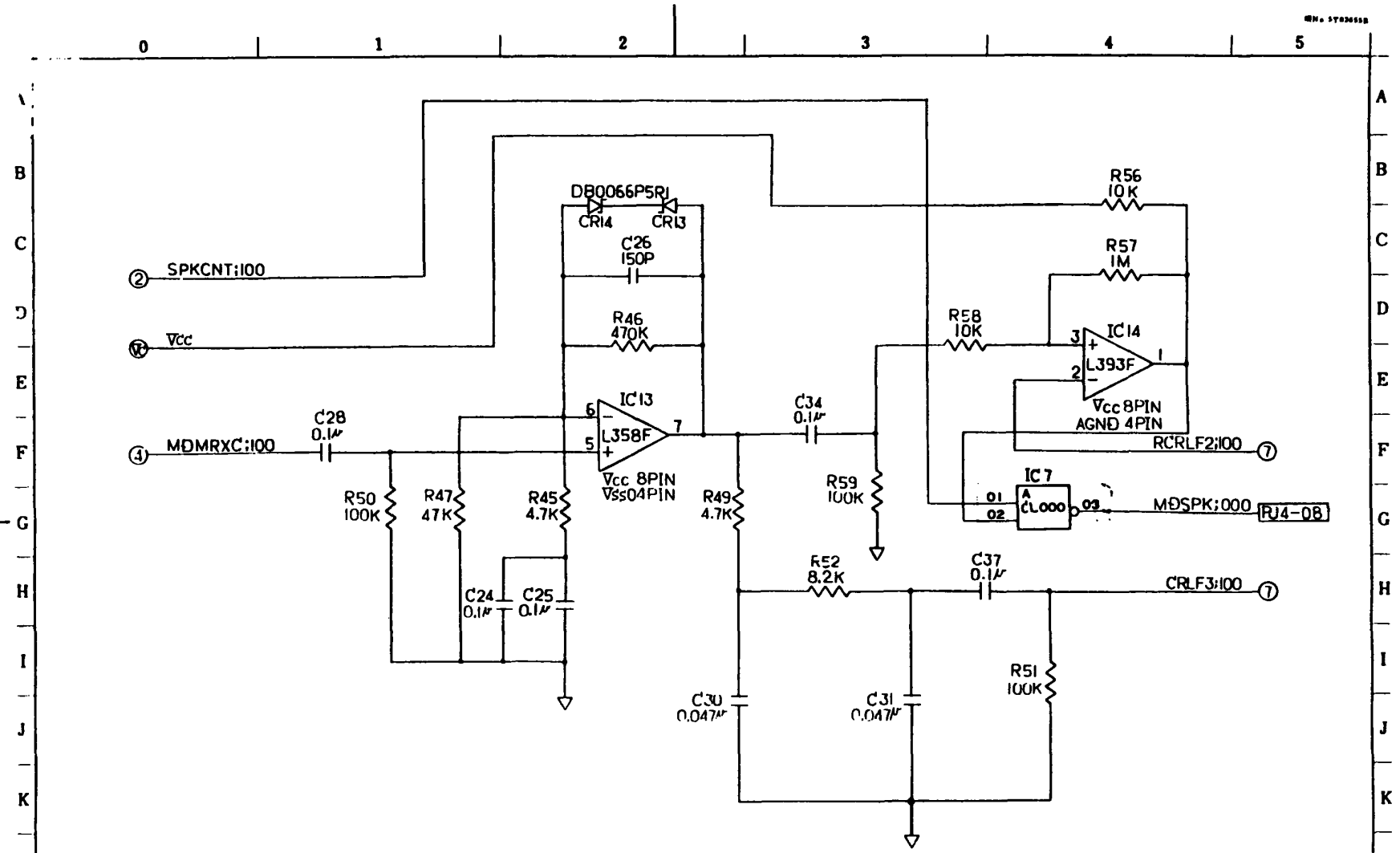
DESIGNED BY	DESIGNED BY	DRAWING DATE	SH. No. 5	DRAWING No.		PAGE No. 8	REV. MARK B

TOSHIBA CORPORATION



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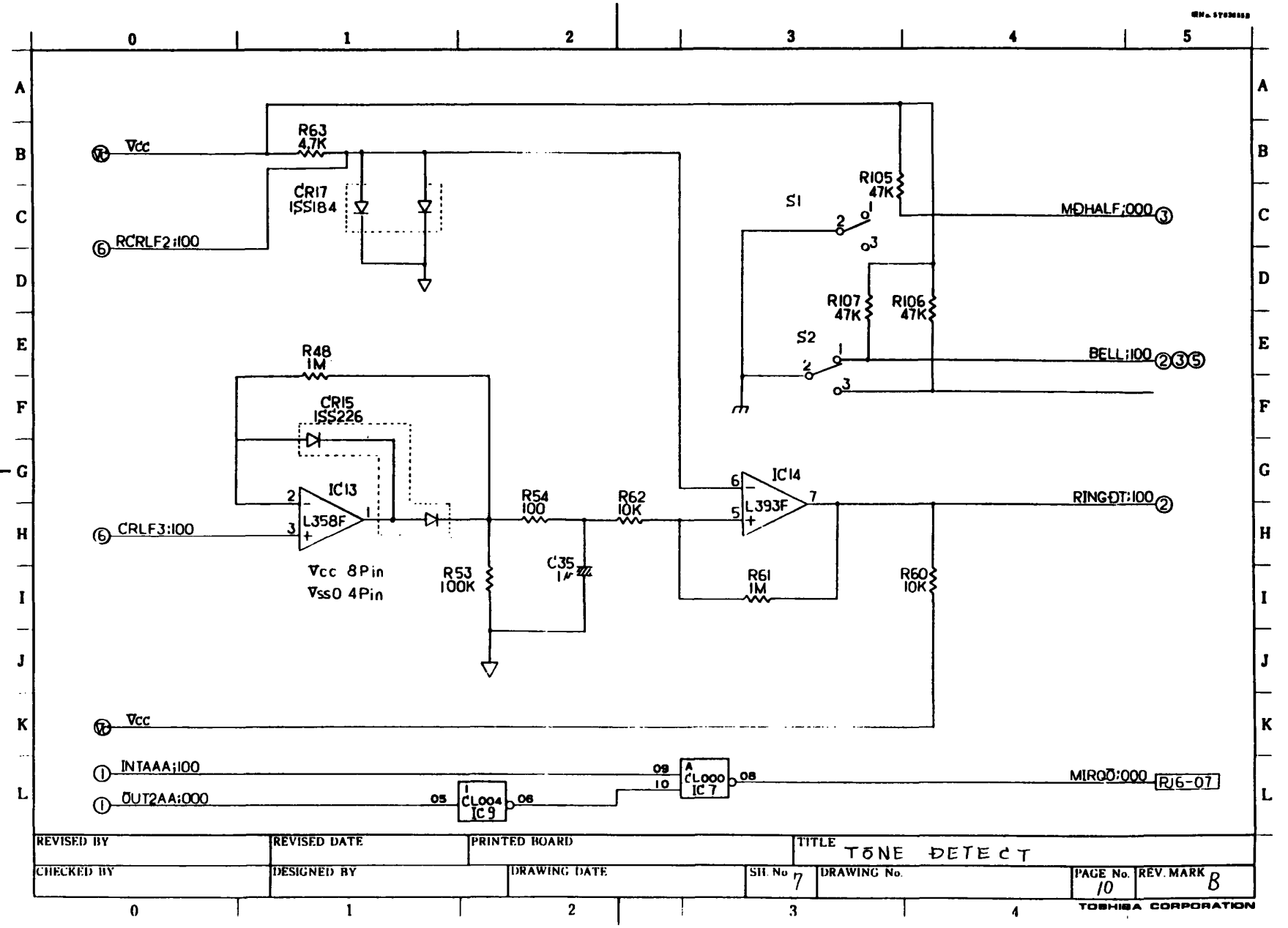
CHECKED BY	DESIGNED BY	DRAWING DATE	SH. No. 6	DRAWING No.	PAGE No. 9	REV. MARK C

TOSHIBA CORPORATION


Vcc
R63
4.7K
CR17
ISS184
RCRLF2:100
S1
R105
47K
MDHALF:000
R107
47K
R106
47K
S2
BELL:100
R48
1M
CR15
ISS226
IC13
L358F
IC14
L393F
R54
100
R62
10K
RINGDT:100
CRLF3:100
Vcc 8Pin
Vss0 4Pin
R53
100K
C35
1μ
R61
1M
R60
10K
Vcc
INTAAA:100
OUT2AA:000
CL004
IC9
CL000
IC7
MIR00:000
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TITLE
TONE DETECT
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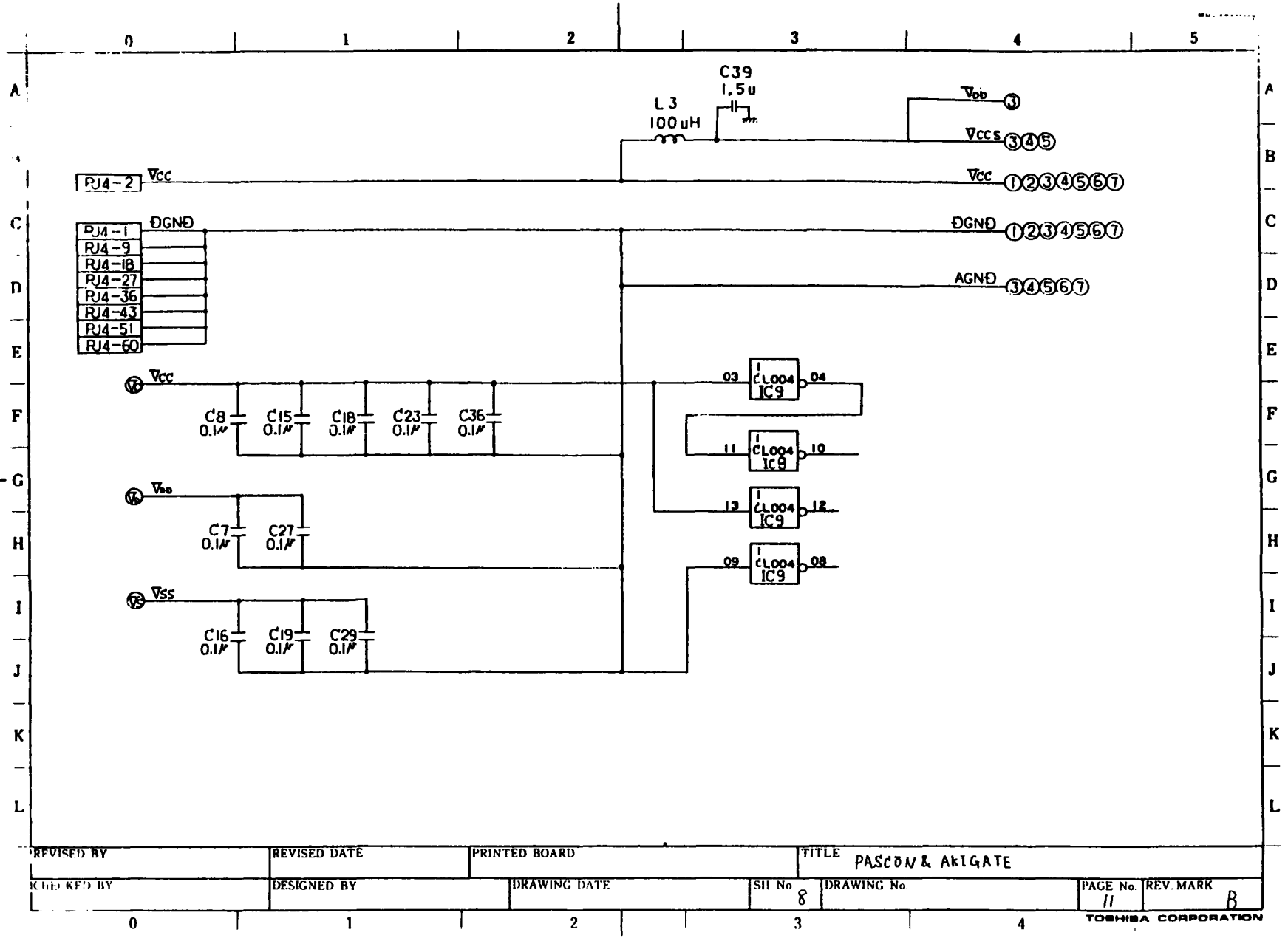
TOSHIBA CORPORATION



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CHECKED BY	DESIGNED BY	DRAWING DATE	SII No 8	DRAWING No.	PAGE No. 11 / REV. MARK B

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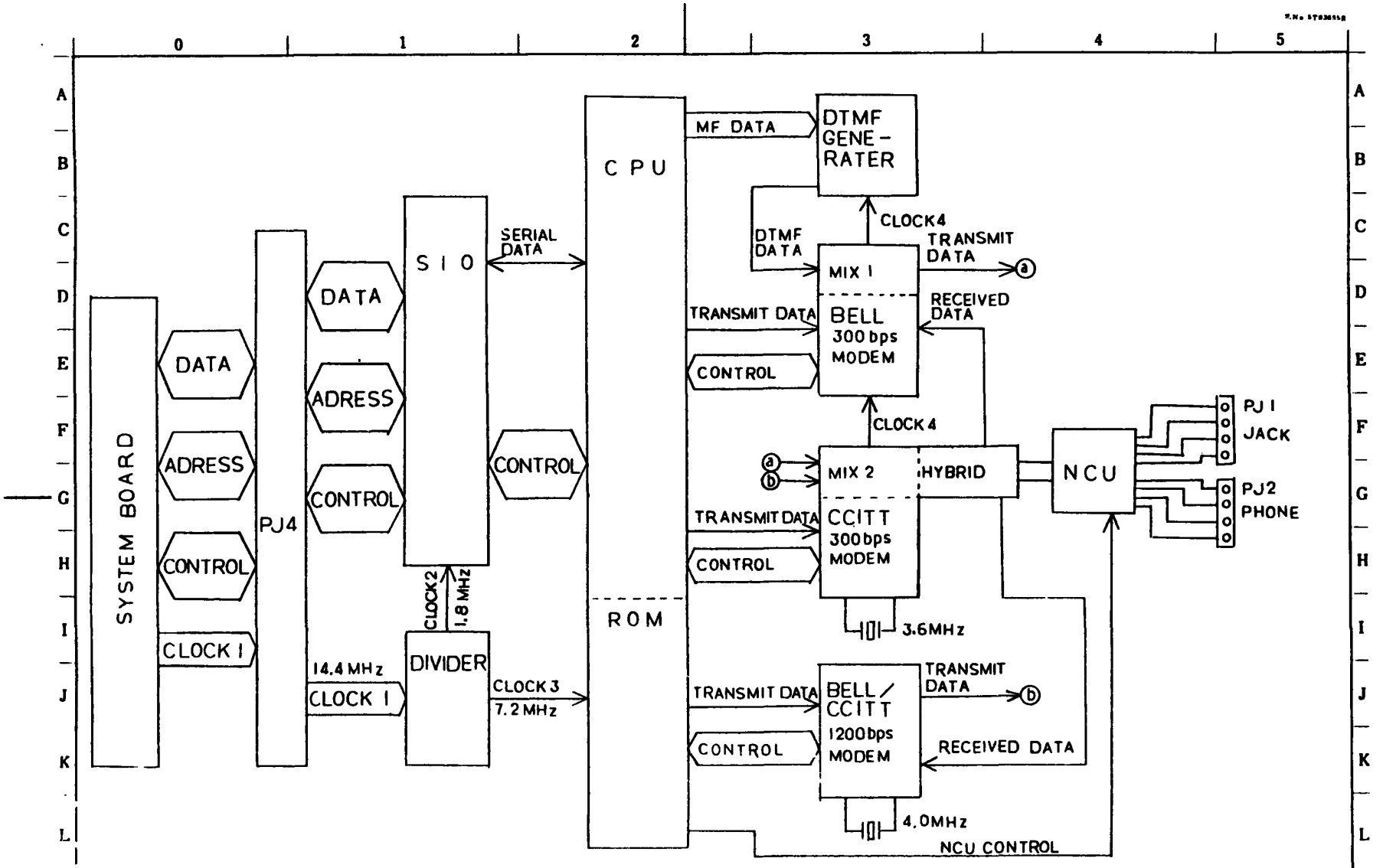

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